Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 25, Number 2, 1991

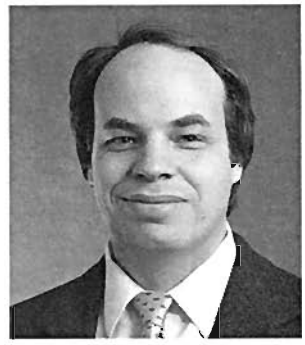
ANALOG DEVICES

Editor's Notes

AVAILABILITY—DISTRIBUTION

In our welcome to Precision Monolithics (PMI) as a new Division of Analog Devices (*Analog Dialogue* 24-3, 1990), we noted that in the North American market their products were sold through distributors. We predicted that the ease of purchasing in any quantity, and the benefits of distributor inventory that this brings to both small- and large-quantity users would be potentially available in the future for many Analog Devices parts in the U.S.A. and Canada. It has already come to pass. Now the Analog Devices line of standard ICs is available through the many branch locations of these distributors: Alliance Electronics, Allied Electronics, Anthem Electronics, Bell Industries, Future Electronics, Hall-Mark Electronics, Newark Electronics, Pioneer Standard Electronics, Pioneer Technologies Group, and Zentronics.

BOB ADAMS: AES FELLOW



We are pleased to note that Robert W. Adams has been named a Fellow of the Audio Engineering Society (AES) "for his significant influence on the theory and practical realization of high-precision oversampling analog-to-digital and digital-to-analog converters and their measurement." According to Dr. Marshall Buck, President of the Audio Engineering Society, "Bob's AES Fellowship is a tribute to his creative, state-of-the-art approach to design of the key component in digital audio engineering, the a/d converter."

Adds Dennis Buss, Analog Devices' Vice President of Technology Development, "Since joining Analog Devices, Bob has undertaken the lead role in developing technically advanced sigma-delta analog-to-digital converters, including the AD1879, which established a new performance benchmark for audio recording applications. Bob continues to define innovative circuit architectures, many presently in development, which promise to further increase digital audio fidelity, and he continues to be an active participant at technical conferences."

Bob Adams joined Analog Devices in 1989 as a Senior Design Engineer for digital audio converter products at Analog Devices Semiconductor Division, Wilmington MA. He works on a diverse range of consumer- and professional audio ICs, including a/d and d/a converters and other high-performance signal-processing devices. The AD1879, an 18-bit sigma-delta ADC for stereo, was described in a paper presented at the 1991 AES Convention in Paris, France.

Adams was born in Syracuse NY and received his BSEE in 1976 from Tufts University, Medford MA. After a brief career as a professional musician, he worked at ADS, Inc., a manufacturer of automotive audio electronics and loudspeakers. In 1977, he joined dbx, Inc., designing oversampling a/d converters for digital audio, and later became Director of Research. Products that his work led to include an early recording system that employed companded delta modulation—and later a 20-bit stand-alone a/d converter using sigma-delta technology.

Bob has published many papers under the auspices of AES and IEEE[1] and holds several circuit patents. He is a Sustaining Member of AES and a Member of IEEE.

Dan Sheingold

[1]Several of his papers are included in the book, *Oversampling Delta-Sigma Data Converters*, edited by Candy and Temes. New York: IEEE Press, 1992.

THE AUTHORS

Pete Predella (pages 12 and 15) is a Technical Publicity Associate at Analog Devices, in Norwood MA. Since joining ADI, in 1979, he has also been a Technician for the Component Test Systems and Memory Devices Divisions. Peter is a graduate of GTE Sylvania Technical School and is currently pursuing a BSET from Northeastern University. His interests include reading, salt-water fishing, and golf.

Joe Buxton (page 19), a Senior Application Engineer for the PMI Division of Analog Devices, has worked extensively on the development of SPICE op amp models; he writes application notes and articles for publication and also helps customers resolve their circuit and design problems. In 1988, Joe received a BSEE from the University of California, Berkeley. In his leisure time, he enjoys bicycling, hiking, skiing, and listening to music.

Bill Schweber (page 3) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*. His photo and a biographical sketch appeared in the last issue of *Analog Dialogue*, 25-1.

James Bryant (page 24) is European Applications Manager for ADI, based in Newbury, England. His photo and a biographical sketch appeared in the last issue of *Analog Dialogue*, 25-1.

COVER DESIGN

The cover illustration symbolizes the compact representation of numbers in a floating-point format. Designed and executed by Shelley Cohane, of Design Encounters, Hingham MA, it incorporates a graphic design copyrighted by Digital Art/Westlight.

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Floating-Point DSP for High-Speed Signal Processing

A fast, easy-to-use descendant of the popular ADSP-2100 fixed-point family, the ADSP-21020 inaugurates a new generation

by Bill Schweber

The recently announced ADSP-21020* expands Analog Devices' family of digital signal processing (DSP) ICs to encompass floating-point operation. Like the well-established fixed-point ADSP-2100A microprocessor and ADSP-2101 microcomputer families,† this device—first of a series of floating-point DSPs—has an architecture optimized for signal processing. It thus combines high attainable performance with ease of use.

PERFORMANCE

The critical measure of a processor for real-time signal-processing applications is *achievable performance*. If a DSP lacks the speed to implement an algorithm in real time, either the processor or the algorithm must be replaced. This contrasts with processors that accelerate computer performance in essentially off-line numerical computations; for these applications, while "faster is better," displaying the answer a little slower than desired (e.g., 4.72 s vs. 4.25 s) is inconvenient but not critical.

There are many ways to specify the performance in terms of device parameters—for example, cycle time, MFLOPS (millions of floating-point operations per second), and clock speed—but these alone aren't especially useful to the system design engineer. Algorithm-performance benchmarks are much more meaningful for signal processing, since they are examples of performance achieved in actual real-time computations.

The 1024-point complex fast Fourier transform (FFT) is often used as a primary figure of merit in signal-processing benchmarks. Table 1 records the ADSP-21020's submillisecond benchmark performance for this algorithm, as well as other common signal processing applications and basic operations.

Table 1. ADSP-21020 Benchmark Performance

ADSP-21020 Grade:	-100	-80	-60	
Operations				Units
Instruction cycle	40	50	60	ns
Complex FFT, 1024-point				
Radix 2 with bit-reverse	0.77	0.96	1.155	ms
N-tap FIR filter (per tap)	40	50	60	ns
Y/X (floating point divide)	320	400	480	ns
$1/\sqrt{X}$ (floating pt. sq. root inverse)	520	650	780	ns
Matrix multiply (pipelined)				
$[3 \times 3] \bullet [3 \times 1]$	360	450	540	ns
$[4 \times 4] \bullet [4 \times 1]$	640	800	975	ns
IIR Filter (per biquad)	200	250	300	ns

*Use the reply card for technical data. Circle 1
†Use the reply card for technical data. Circle 2

OVERVIEW

Like the fixed-point DSPs, the ADSP-21020 (Figure 1) supports the five prime requirements for digital signal processors[1]:

- *fast, flexible arithmetic units:* the ADSP-21020 executes all instructions in a single cycle

[1]"Application decides optimal DSP architecture," by Bob Fine and David Fair, *Analog Dialogue* 24-1 (1990), pp. 9-11.

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- *unconstrained data flow to and from the computation units:* the Harvard architecture is supported by a 10-port register file. In every cycle: two operands can be read or written off-chip to or from the register file; two operands can be supplied to the ALU; two operands can be supplied to the multiplier; and two results can be received from the ALU and the multiplier (three, if the ALU operation is a combined addition/subtraction)
- *extended precision and dynamic range in the computation units:* the processor uses IEEE-standard floating-point format (user-chosen 32- or 40-bit), and all extended-precision results are carried throughout its computation units, to avoid overflows and limit intermediate data-truncation errors.
- *dual address generators for program and data memories:* they provide both immediate and indirect (pre- and post-modify) addressing; they also support modulus and bit-reverse operations vital to effective execution of algorithms such as the FFT.
- *efficient, zero-overhead program sequencing and control:* in addition to zero-overhead loops, the ADSP-21020 supports single-cycle setup and exit for loops; loops can be nested (up to six levels in hardware) and interrupted.

The ADSP-21020 extends these features as necessary for a floating-point version (see adjacent box) and easier system development. The enhancements embodied in the ADSP-21020 are primarily in four categories: *high-level language support*, *JTAG serial scan-path access*, *IEEE-standard floating-point operation*, and *open memory architecture*. These features distinguish the ADSP-21020 from other floating-point DSPs (or fast microprocessors) available today.

High-level languages (HLLs) have the potential to provide many benefits to the system designer and programmer via more-structured code, fewer bugs, use of available algorithms, and even use of the same code on processors from several vendors. Their disadvantages have been that HLLs usually compile inefficiently, producing cumbersome machine code that takes more time and occupies more memory than well-tuned assembly language.

To overcome these disadvantages by supporting compact compiled HLLs and fast execution, the ADSP-21020 family architecture features:

- general-purpose data- and address register files, which can be flexibly used by the compiled code.
- 32-bit native data types [e.g., integer, floating-point, etc.], so that internal number format is consistent and efficient.
- large address spaces: 16 megawords for program memory, 6 gigawords for data memory.
- pre- and post-modify addressing formats
- unconstrained placement of the circular buffer in data memory
- on-chip *program*, *loop*, and *interrupt* stacks.

In addition, the ADSP-210XX family is designed to support *Numerical C*, an extension of ANSI C. Numerical C is a compiled language; it supports vector data types and operators for numeric and signal-processing applications.

JTAG serial scan-path access implements an IEEE standard method for serially scanning the I/O status of each component in a system. Besides allowing the manufacturer to test ICs more easily, quickly, and thoroughly, JTAG has major impact on emulation (see *development tools*, page 7).

Floating-point support: Any processor, whether fixed- or floating-point, can produce results with sufficient resolution via careful

WHICH FLOATING POINT?

Floating point is simple in concept; but its actual implementation for practical computation with binary words of fixed length is not. The many special cases and exceptions that must be handled include: truncation, roundoff, overflows, underflows, divide-by-zero, etc. An IEEE Standard (IEEE 754/854) for floating-point numerical processing fully defines how numbers are to be formatted and handled, including rules for handling exceptions.

The ADSP-21020 implements the IEEE standard in 32- and 40-bit floating-point formats. It also implements 32-bit fixed-point and fractional formats. The MAC's accumulator has a fixed-point format (which is a subset of the floating-point standard) with an 80-bit capacity to allow for significant overflows in true 32-bit fixed-point computations.

Support of the IEEE standard has a significant benefit for the ADSP-21020 user: algorithms can be ported between various platforms. For example, an algorithm can be developed, fine-tuned, and validated on a workstation, then ported to a system. The identical results will occur if the system platform and software also support the standard. On the other hand, results can differ significantly when one or the other platform does not support the standard; biased rounding and differences in exception handling can build up errors through repeated executions of arithmetic operations.

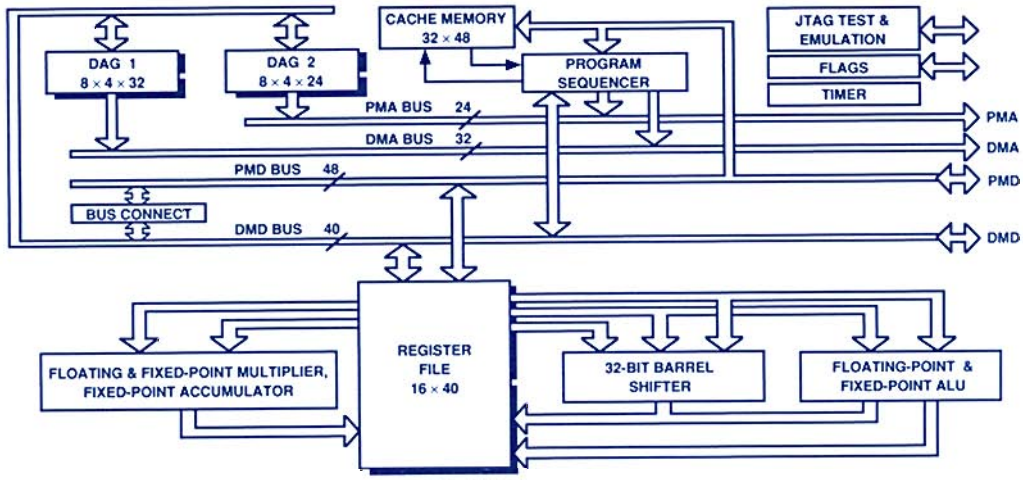


Figure 1: ADSP-21020 block diagram.

algorithm structure, manipulation of the numbers, and numerical analysis. For example, an 8-digit, fixed-point calculator can produce results with more than 8 significant figures if the user breaks the calculation into parts, performs scaling and descaling, etc. Though usable, fixed-point format can result in inefficient coding and execution. Thus, as users employ higher-speed- and -resolution a/d converters, a fixed-point DSP becomes more difficult to program effectively for real-time applications.

Floating-point processors are easier to use in equipment design, allowing a quicker time-to-market than processors that do not support the format. In fixed-point operation, the programmer (or compiler) must carefully scale, observe range restraints, and be alert for the inevitable scaling and ranging errors. Some estimates indicate that fixed-point scaling, ranging, error handling, and debugging can take 30% of the programmer's time.

Floating-point data formats easily extend the precision and dynamic range of DSP and permit a wider range of algorithms to be used. Many algorithms (such as those used in compression and decompression of digitized analog signals, or for speech recognition) were originally developed to operate on well-behaved signals bounded by many constraints. The present trend toward increased flexibility, with fewer constraints on the behavior and dynamic range of the intermediate results of the algorithm, necessitates floating-point operation. Examples include adaptive filtering, image processing, and more general voice-related applications. Other applications with low signal-to-noise ratios, such as radar and sonar, need wide dynamic range to process accurately the many computational steps required to extract signals from noise without accumulating excessive error.

But fixed-point DSPs are by no means dead. They are inherently less expensive and consume less power—and are well-suited for applications needing less precision or with properly bounded signals, as in modems and other voice-band applications.

Open memory architecture: The ADSP-21020 is designed to handle large amounts of memory *off chip*. This is done to avoid the constraints that limited on-chip memory imposes on the development and upgrade of floating-point algorithms for signal processing. It also facilitates the use of high-level languages and multitasking operating systems. An on-chip high-performance cache, operating with two data-address generators, enables parallel access to two off-chip memory spaces on every cycle.

ARCHITECTURE

There are three independent computation units (Figure 1): an arithmetic-and-logic unit (*ALU*), a *multiplier* with fixed-point accumulator (*MAC*), and a *shifter*. The units are connected in parallel (not serially) and the output of any unit on one cycle can be the input of any unit on the next cycle. A 10-port *register file* is used for transferring data among computation units and data buses, and for storing intermediate results.

The ADSP-21020, like the fixed-point ADSP-2100 family, has a *Harvard architecture*, which provides for two independent memories—one for *data*, the other for *program instructions and data*. Within the DSP there are *two independent address generators*; one supplies a 32-bit address for data-memory data; the other provides a 24-bit address for program-memory data. A *program sequencer with a 32-word instruction cache* allows the ADSP-21020 to access data from both data memory and program-memory *and fetch an instruction*—in the same cycle, without any delay.

There are five external hardware *interrupts*, eight software interrupts, and nine internally generated interrupts. Interrupt service requests can be nested up to four deep. Many of the registers in the ADSP-21020 have *alternate registers* (shadows) which hold duplicate data; they retain the existing data during interrupt servicing when context is switched. A *programmable timer* provides periodic interrupts, counting down from a 32-bit count register (automatically reloaded).

The ADSP-21020 is built on a 200 × 200-mil die with 300,000 transistors (Figure 2) and is housed in a 223-lead plastic pin-grid array package. Two grades are available: -80 (50-ns instruction cycle) and -60 (60-ns); and a third, -100 (40-ns) is now available in sample quantity. Prices for -80 and -60 (1s) are $265 and $195.

The ADSP-21020 was designed by a team headed by Doug Garde, at Analog Devices' Norwood, MA, DSP facility.

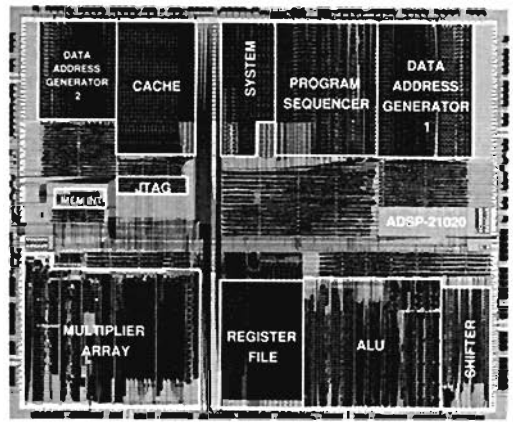


Figure 2: ADSP-21020 chip microphotograph.

AdSP-21020 vs. PIPELINED PROCESSORS

For repetitive computations, pipelined architectures can increase overall performance by allowing one instruction to be executed, while the next instruction (or instructions, depending on the length of the pipeline) is fetched and decoded. Similarly, data is pipelined to increase throughput.

For applications with predictable program flows, such as digital filtering, pipelines give the benefits of higher effective throughput without proportional speedup in processor cycle time. Other applications include many-step, deterministic numerical algorithms common in equation-solving.

But pipelines can have the opposite effect in many signal-processing applications. Every time the program diverts from a normal linear flow—such as at the end of a loop (or nested loops), or when an exception or out-of-bound condition occurs—the program must jump to a new code sequence. To do this, the now-incorrect numbers that resulted from previous instructions must be "flushed out" of the pipeline.

This latency wastes processor cycles and negates any benefit the pipeline may have provided. It's especially apparent in such applications as matrix inversion, which has a regular computational structure but often generates exceptions (overflow, underflow). Pipelines also make programming more difficult, since data flow within the processor must be carefully tracked.

The ADSP-21020 achieves its performance without the use of an internal arithmetic pipeline; all *numeric* operations are completely executed within a cycle, leaving no intermediate data. Instructions require three steps (fetch/decode/execute) and can be pipelined.

Numerical C Speeds Code Development and Execution

High-level language is tailored for vector and matrix arithmetic, critical in signal processing

The major reasons for a system designer to use a high-level, standardized programming language are ease-of-use, portability between platforms, maintainability (ease of modifying a program), and time-to-market for the user's end product. Three variations of the popular C high-level programming language are attracting the attention of DSP systems engineers—"standard" C, Numerical C, and C++. ANSI Numerical C, a language that addresses the implementation of signal and numerical processing, is the most interesting, since it efficiently handles vector and matrix data, frequent subjects of signal-processing algorithms. Analog Devices has named its Numerical C compiler DSP/C™.

THE C PROGRAMMING LANGUAGE

C was created in the 1970s at AT&T's Bell Labs. Its generality, and the easy portability of C programs between hardware and operating system platforms, caused its popularity to grow for diverse applications on many machines and embedded systems.

Compared to many other HLLs, C is fairly "low-level" in that it understands a small set of basic objects (integer and floating-point data types) and manipulates them with an equally basic set of logical and arithmetic operations. As a result, it is relatively "small" and provides a solid foundation upon which more-complex objects and more-powerful operations may be built. It provides facilities, such as structure definitions, unions, arrays, etc., for defining objects beyond the basic set; and ramified operations may be implemented in functions defined by the user or contained in libraries.

During the 1980s, because of the growing popularity of C and the virtues of standardization, ANSI (American National Standards Institute) formed the X3J11 committee to prepare a draft standard for the C language. Besides the language itself, the committee proposed a set of standard library functions that provide the programmer with higher-level functions for performing input/output, storage allocation, control, and mathematical operations (such as sine and cosine). Many of today's C compilers come with libraries of these "standard" functions; other libraries provide functions for special purpose applications such as graphics, serial communications, and DSP.

NUMERICAL C

Numerical C, an upwardly compatible superset of Standard C, is currently being drafted as an ANSI Standard, X3J11.1, slated to be published for comment in 1992. It will aid software developers for signal-and numerical processing by adding vector data types and vector operator extensions to the C language.

Numerical C allows vector and matrix algorithms to be expressed in a natural way and efficiently compiled to match the vector capability of a processor. This language is especially effective if the target processor is a DSP that contains hardware support for both fast arithmetic and vector addressing & manipulation—like the ADSP-21020. With the Analog Devices DSP/C compiler, which supports Numerical C on the ADSP-21020, the HLL compiles directly to the processor instruction set. The result is optimal treatment of looping, pipelining, parallelism, and array addressing. It also incorporates DSP data types such as complex numbers ($a + bj$), and fractional numbers (1.31, for example).

It can simplify programming in such new functional areas as unary vector-sum and vector-product, and binary dot-product & autocorrelation. These functions permit operations such as matrix multiplication to be specified with *a single line of code* instead of a series of nested loops. Table 1 gives an example comparing C and Numerical C. The availability of additional data types such as *complex* and *fract* also simplifies coding of DSP algorithms.

Table 2 shows an example of DSP/C and the resulting compiled ADSP-21020 assembly language. Other extensions to ANSI Standard C included in Numerical C will allow compilers to perform optimizations as effective as those achieved with optimizing Fortran compilers. All major DSP vendors are developing Numerical C links to their chips; Analog's DSP/C, scheduled for production release in early 1992, is one of the first.

The Numerical C development team at Analog Devices is headed by Kevin Leary.

DSP/C solution:

```
mvmultiply()
{
    y[:] = A[:][:] * x[:];
}
```

ANSI C solution:

```
mvmultiply()
{
    int i,j;
    int sum, inca;
    for (i =  0;  i< nrA; i++)  /* column */
    {
        inca = i * ncA;
        sum = 0.0;
        for  (j= 0 ; j < ncA ; ++)  /* row */
             sum += A[inca + j] * x[j];
        y[i] = sum;
    }
}
```

Table 1. DSP/C™ and ANSI C source code compared: matrix vector multiplication example.

DSP/C program statement:

```
float delay[N], *circ delay_ptr, c[N];

fir_filter()
{
    output=sum(delay_ptr[:]*c[:]);
}
```

Compiler-generated assembly code

```
FirFilter_:
                    Array selection operator determines
    i0=coef;        start addresses, stride, and loop count
    f9=0.0;
    f1=0,f4=dm(i0,m0),f5=pm(i8,m8);   "do" instruction sets up do
    lcntr=4, do lll until lce;        loop for no-overhead looping
lll:  f1=f1+f9,f9=f4*f5,f4=dm(i0,m0),f5=pm(i8,m8);
    f1=f1+f9;
    rts;
                    DAG automatically updates Ireg and
                    performs modulo operation
```

Table 2. DSP/C and ADSP-21020 assembly code generated by compiler: FIR filter example. Note similarity of assembly code to mathematical operations to be performed.

Development Tools and Third-Party Support for Floating-Point DSP

Industry-wide support for ADSP-21020 includes hardware, software, and algorithm development

Successful development of a processor-based product requires more than just the processor and its data sheet or User Manual. Effective development tools and third-party software and hardware support are critical, especially in the algorithm-intensive applications of digital signal-processing.

The available development tools for the ADSP-21020 are similar to those for the fixed-point family, but extended as required for floating-point. The software tools for the coding and debugging environment (Figure 1) are available in a PC-based development software package, the ADDS-210XX-DSW-PC. A Sun-platform version will be available soon.

The *Macro assembler* creates object files from the processor's assembly source code in the form of relocatable COFF (Common Object File Format) files. It accepts conditional assembly directives, as well as macro and listing directives, as part of the source file. The algebraic syntax (similar to that for the fixed-point ADSP-2100 family) facilitates coding of DSP algorithms.

The *Linker* processes separately assembled object files to create a single executable program. It assigns memory locations to code and data in accordance with a user-defined architecture file that describes the memory and I/O configuration of the target system. Input to the Linker consists of one or more object files in COFF format produced by the ADSP-210XX family Assembler and/or Library files. The *Librarian* allows the user to group frequently used object files into a single library file for input to the Linker.

The *Simulator* executes an ADSP-21020 program in *software* in the same way that an ADSP-21020 processor would in *hardware*. It provides a window-oriented graphical user interface (GUI), an extension of the one used by the improved ADSP-2100-family simulators. Most commands are accessed from pull-down menus with a mouse. Input to the Simulator consists of an executable file produced by the Linker—and an architecture file, to simulate a specified memory and I/O configuration.

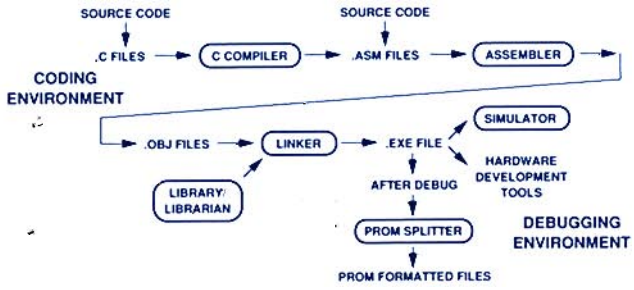
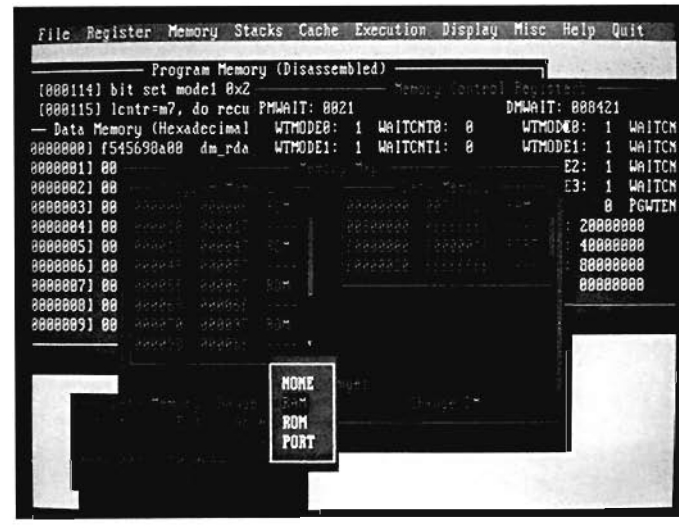


Figure 1: Programming environment.



The *PROM Splitter* reformats an executable program into files that can be read by a PROM programmer. PROMs can then be programmed for use in the user's ADSP-21020 system.

The Development Software package, bundled with the optimizing C Compiler and Runtime Library (ADDS-210XX-BUN-PC) includes the Assembler, Librarian, Linker, Simulator, and PROM Splitter described above. It also includes an ANSI C compiler, which complies with the ANSI specification—as verified with the Perennial and industry-recognized Plum-Hall validation suites. Offering a variety of options for optimization and runtime support, it takes advantage of the ADSP-21020 high-level-language-compatible architectural features. It also comes with a runtime library of over 100 standard and DSP-specific functions.

Hardware support: The EZ-ICE™ Emulator (ADDS-21020-EZ-ICE) provides the DSP system developer with a low-cost software debug environment that allows non-intrusive access to the internal ADSP-21020 registers via a JTAG interface (see box). The use of on-chip emulation features allows the EZ-ICE to emulate any target system reliably.

The EZ-LAB™ Evaluation Board (ADDS-21020-EZ-LAB) (Figure 2) is a complete, general-purpose, stand-alone ADSP-21020 system with program and data memory. It also features analog I/O via codecs—A/D and D/A converters, to provide a complete analog-to-DSP-to-analog signal processing system. The download path from the PC enables the user to download and run user-developed and other programs directly on the EZ-LAB™. When used in conjunction with the EZ-ICE Emulator, it forms a powerful software debugger.

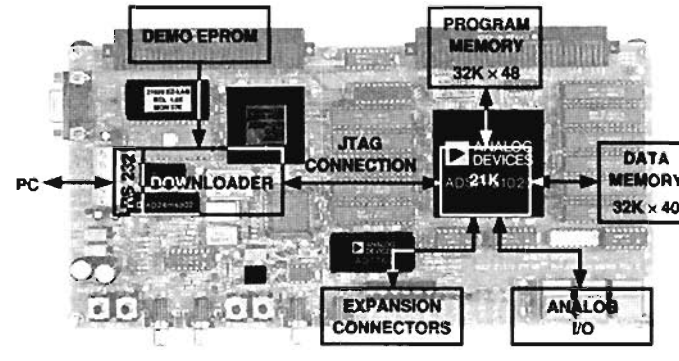


Figure 2: Block diagram of EZ-LAB.

THIRD-PARTY SUPPORT

No single DSP vendor can provide the variety of software and hardware support to meet the needs of all users. To help satisfy the diverse and specialized needs of ADSP-21020 users, Analog Devices has worked with various third party vendors to provide additional tools.§ Here are some examples:

- **Spectron Microsystem: SPOX Operating System**

The SPOX real-time DSP operating system provides a real-time kernel and libraries that enable software developers to work with objects relevant to signal processing such as vectors, filters, and streams. In addition, SPOX addresses the broader needs of real-time system designers through general-purpose features such as device-independent I/O, interrupt management, and multi-tasking support.

Spectron's recently announced OSPA—an Open Signal Processing Architecture— defines a robust set of CISC or RISC-to-DSP communications protocols, which will standardize the host-to-DSP interactions in applications ranging from imaging and audio to multimedia workstations.

Combined with powerful high-level languages, like ANSI's Standard C and Numerical C, Spectron's products provide for portability of DSP application software across a wide variety of processors and hardware platforms. Simplifying applications development, they also preserve a user's investment in code development.

- **Comdisco: Signal-Processing Workstation**

The Signal Processing Worksystem, for development of signal processing applications at the systems level, is an environment that provides integrated and interactive design, simulation, and implementation for the development of DSP and communications systems.

Comdisco's Code-Generation System can generate C code linked with efficient assembly-language routines targeted for the ADSP-21020. Using the Signal-Processing Workstation, designers can move quickly from high-level system design to actual, in-place code on the DSP processor.

- **LSI/SSP: PC plug-in System Board**

This IBM PC plug-in board from *Loughborough Sound Images/ Spectrum Signal Processing* includes an ADSP-21020 and up to 640 K words of both program and data memory. Like other Loughborough products, the System Board has a DSP-Link expansion port and two channels of 16-bit analog I/O. The software interface to the board is through a user-friendly Windows 3.0 debug monitor.

- **Momentum Data Systems: FDAS Filter Design and Analysis System**

FDAS combines a filter-design package with system analysis software. IIR filter designs include Butterworth, Chebyshev, and Bessel characteristics. FIR filter designs include window functions. The system-analysis features allow transfer function characteristics to be determined, including: magnitude, phase, group delay, log magnitude, impulse response, and pole/zero locations. The FDAS system is available with source code generation for the ADSP-2100 and −2101 fixed-point DSPs, and ADSP-21020 floating-point DSP; it generates files to interface to the Spectrum/ Loughborough system boards supporting these processors.

§For information on how to get in touch with these vendors, call Analog Devices DSP Applications, at (617) 461-3672. Or circle 3

- **Hyperception: Hypersignal Workstation.**

This is an integrated DSP software package for filter design, simulation, and real-time analysis, generating source code for the ADSP-2100, −2101, and −21020. Processing and analysis software includes FIR/IIR filter design, math functions & signal arithmetic, and FFT processing. Hypersignal-Workstation works with the Loughborough/Spectrum system boards to create real-time functions and PC-based instrumentation—including a dual-channel digital oscilloscope & spectrum analyzer with continuous data acquisition.

The single-user price for ADDS-210XX-DSW-PC development software for the PC is $995; ADDS-210XX-BUN-PC with C compiler is $2195; the EZ-ICE™ Emulator is $2995 (Spring, 1992); and the EZ-LAB™ Evaluation Board is $995.

EZ-ICE Emulator efforts were led by Russ Rivin and Chris Russell; EZ-LAB Evaluation Board design was led by Steve Cox and Kapriel Karagozyan; Development Software by Dave Lannigan and Michael Allen; C compiler by Steve Kafka and Marc Hoffman; Runtime Library by Gordon Sterling and Josh Kablotsky; Development-Tool Engineering is led by Kevin Leary.

JTAG AND EMULATION

IEEE Standard 1149.1 is a boundary-scan technique developed by the Joint Test Action Group (JTAG). The primary purpose of this standard is to make it easier to test systems—both high-density PC boards and ICs—via a "probeless" technique. The basic test bus comprises just four signals: Test Data In, Test Data Out, Test Mode Select, and Test Clock; the Standard also defines additional optional lines.

In the ADSP-21020, JTAG circuitry within the IC is accessed for emulator support via a connector from the IC to the edge of the EZ-ICE™ Emulator's PC board. The JTAG feature—significant among floating-point DSPs—permits the emulator to access all registers and states of the ADSP-21020, to write to and read from external memories, and—not just performing passive monitoring—to take control of the IC, with no degradation of target timing. Thus JTAG builds inherent emulation into the DSP IC, simplifying the design of EZ-ICE, which need not be a large, complex add-on emulator.

Contrast this with a conventional plug-in emulator:

- the plug-in emulator is electrically intrusive: it affects critical timing, loading, capacitance
- full-speed emulation requires fast memory to avoid wait states (by the way, emulators for the fixed-point ADSP-21XX series are indeed full-speed)
- its mechanical structure is often unreliable or awkward
- it is relatively costly.

Though a trace function is not available, the benefits of JTAG emulation in capability, fidelity, reliability, and cost are significant for processor users who must emulate as part of the debug cycle.

References:

"Adding testability also aids debugging," *EDN*, August 2, 1990.
IEEE Standard 1149.1 Designer's Reference, High-Performance Systems, August 1989.

Single-Supply In-Amp for Automotive Applications

Rugged AD22050 has wide common-mode range, meets automotive supply-voltage range and protection specs

The AD22050* monolithic instrumentation amplifier is one in a series of products designed to survive and maintain precision despite the environmental rigors of automotive applications. In the last issue, we described the AD22001† "bulbwatcher," which senses lamp and indicator failures; our next issue will feature a unique surface-micromachined accelerometer IC with precision on-chip signal conditioning and test facilities.

The AD22050 (Figure 1) is a single-supply differential amplifier with an accurate factory-programmed gain of 20 V/V. Its midscale ("zero") point can be set accurately via an Offset terminal—a necessity for bipolar signals in single-supply circuitry. In automotive applications, the device is useful for sensing current (via voltage across low-resistance shunts) in motors, solenoids, and valves—as well as for interfacing and conditioning output signals from pressure transducers, position indicators, strain gages, and other low-level signal sources.

Consisting of a subtractor with gain of 10 V/V and a follower with gain of 2, its accurately preset overall gain is 20 V/V. The gain can be modified with external circuitry to provide any gain in the range from 1 to 160 V/V. Besides its internal transient-spike protection and RFI filtering, the user can readily provide up to 3 poles worth of low-pass filtering with simple external circuitry.

Figure 2 shows a typical application circuit, in which the AD22050 measures the average current through a solenoid, which is pulsed on and off. The average input voltage across the measuring shunt is of the order of 100 mV, while the common-mode voltage ranges from about 1 V above ground—when the transistor is saturated—to about 1.5 V above the battery voltage, when the transistor is cut off and the diode conducts. If the battery voltage spikes up to +20 V, the common-mode voltage can be as high as 21.5 V, which can be readily handled by the AD22050, even with a +5-volt supply.

To measure current with floating shunts, an instrumentation amplifier must be able to handle a wide range of common-mode voltage (CMV) with high common-mode rejection (CMR) and low drift. The AD22050 has a common-mode range of from below ground to $6 \times (V_S - 1.0\ V)$, with performance specified for a +24-volt minimum (and −1.0-V maximum) CMV range with a +5-V supply. CMR is a minimum of 80 dB for low frequencies and 60 dB at 10 kHz. Offset voltage, referred to the input, is a maximum of ±1 mV at +25°C—and ±3 mV over the specified −40 to +125° operating temperature range. Default gain is 20 V/V ± 0.5% at +25°C, and ±1% over temperature.

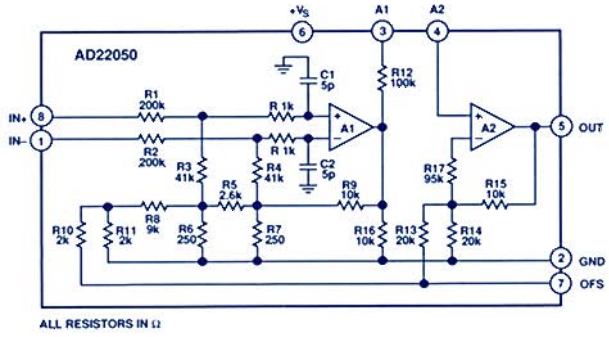


Figure 1. Simplified schematic diagram.

An amplifier for automotive applications must be capable of operating (or at least surviving) over a wide range of supply-voltage variation. The AD22050 will operate at supply voltages from +3 V to +36 V and will survive a reverse supply voltage of −34 V. Its output can be indefinitely shorted to ground, and the device will survive a peak input voltage of 60 V for 40 ms. It is packaged in 8-pin plastic DIPs and SOICs and can be stored at temperatures from −65°C to +150°C. Price begins at $3.90 in 100s, and is typically $1.80 in automotive quantities.

The AD22050 was designed by Analog Devices Fellow Barrie Gilbert for ADI's Automotive/Sensors Group in Wilmington MA.

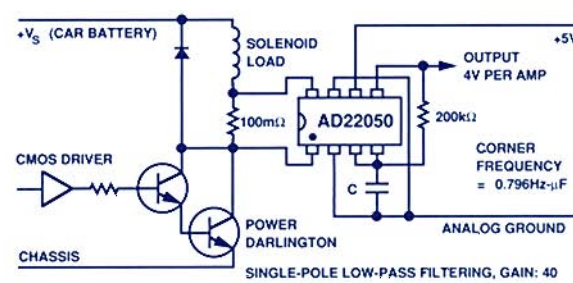


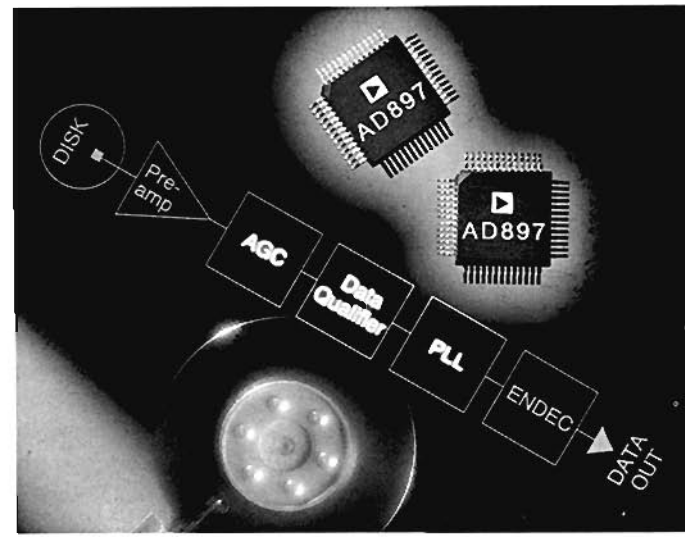
Figure 2. Typical application—current-sensor interface.

*For technical data, use the reply card. Circle 4

†For technical data, use the reply card. Circle 5

Disk-Drive ICs—Optimized for Read-Channel and Servo Loop Control

Read channel: AD897 integrates peak detector, data synchronizer. *Servo loop:* Single-chip AD7774 provides multichannel analog I/O



Hard-drive head circuitry has two major analog paths (Figure 1): the head-positioning control-servo loop and the read/write signal path (called the *read* channel, because most of its circuitry is for recovery of data from the disk). Two new monolithic IC chips are designed to meet these needs. The AD897 provides many of the functions of the read/write path; and the AD7774 Analog I/O Port contains a combination of analog/digital and digital/analog converters designed to meet the needs of the servo control path.

READ CHANNEL: THE AD897

The AD897* (Figure 2) is the newest descendant of the AD890 & AD891 (*Analog Dialogue* 22-1, 1988). The *read* channel, a sophisticated signal recovery-and-detection path, must amplify a low-level, noise-corrupted signal with widely varying amplitude and noise level (due to the mechanics of the disk). The recovered signal must then be qualified as valid data using a variety of criteria and a suitable clock (recovered from the data bits).

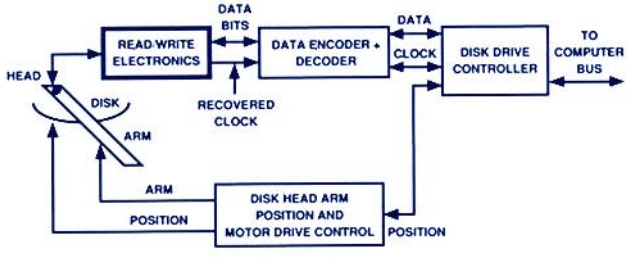


Figure 1: Block diagram of a disk-drive system.

For an input signal from the head preamplifier, the AD897 provides signal conditioning, data qualification, and data synchronization at rates up to 40 megabits per second. It provides a 24-dB-gain buffer, a variable-gain amplifier (VGA) with up to 30 dB of gain—automatically set by an automatic gain-control loop (AGC) having 40 dB of gain range and programmable attack and decay times. The device provides three levels of data bit qualification—and a phase-locked-loop (PLL) for extracting bit timing from the data bits. The IC provides for external filters, configured by the user to match the data rate, media characteristics and other system requirements.

The AD897 qualifies data by amplitude threshold, time above amplitude threshold, and data polarity to ensure minimum *bit error rate*, a key system-level spec for drive *read* channels.

Amplitude (level) qualification is performed in level-comparators by comparing the normalized signal with a user-set threshold. Each comparator then drives a resettable delay line, to effect the "time above threshold" qualifier. After the recovered signal has been validated by these first two criteria, a comparator is used to detect differentiator zero crossings and clock a flip-flop if the

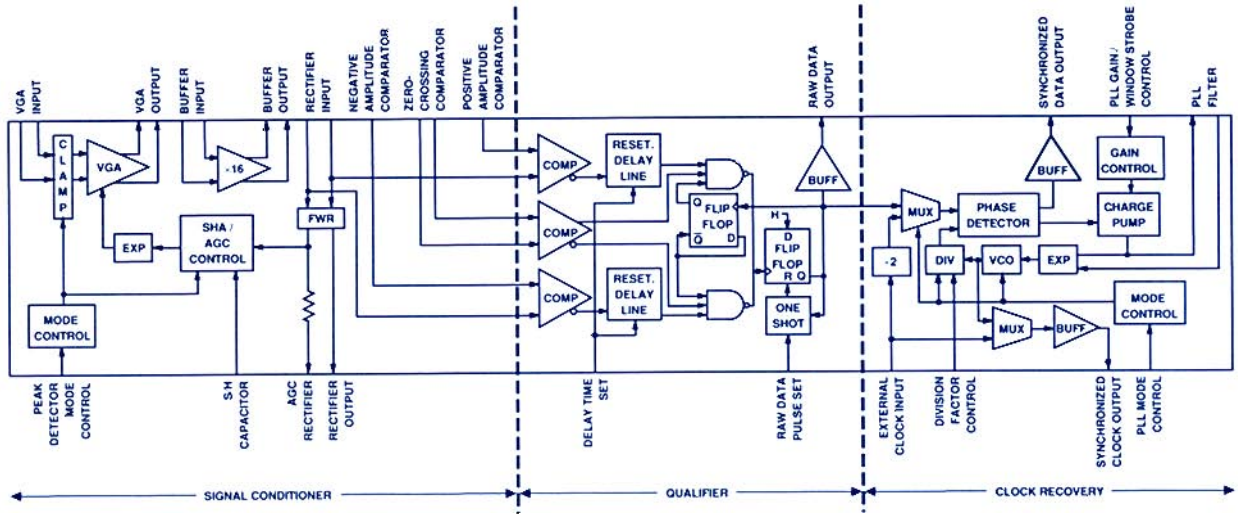


Figure 2: AD897 functional block diagram.

*For technical data, use the reply card. Circle 6

†For technical data, use the reply card. Circle 7

signal has the correct polarity. The validated data event triggers a one-shot to produce the final, validated, timed data pulse—of width set by an external resistor. Figure 3 shows the operation of the qualifier for RLL 1,7 code (the most demanding); the AD897 also handles standard codes such as MFM and RLL 2,7.

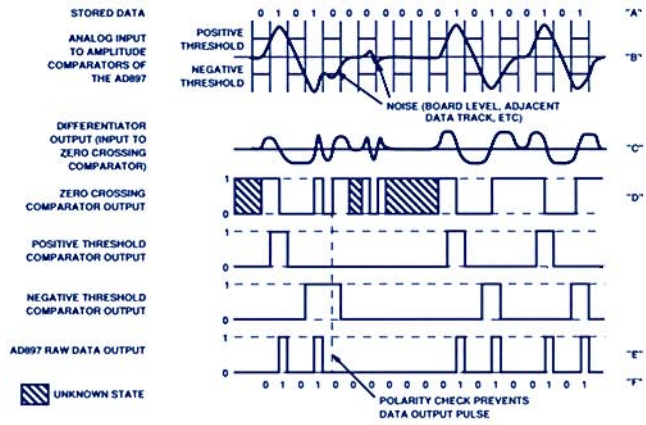


Figure 3: AD897 Operation.

A key feature of the AD897 is the dead-zone-free data synchronizer PLL; it has four modes of operation: external clock, lock-to-data-preamble (frequency lock), lock to data (phase lock), and a three-state (*coast*) mode which holds the loop's filtered error voltage with low droop and avoids transients during mode switching. The three-state mode is useful when the *read* head is jumping across areas of the disk and there is no data to lock onto.

Performance: Besides its 40-Mb/s data transfer rate capability, the AD897 features 500-ps maximum additional pulse pairing and 0.1-dB/ns gain drift in the *coast* mode. The PLL has ±1-ns maximum window uncertainty, and no VCO startup phase error. The AD897, packaged in a 52-pin quad flat pack, will operate at temperatures from 0 to +70°C. Its high-volume price is $7.50.

SERVOLOOP: AD7774

The monolithic AD7774† combines (Figure 4) multiple channels of a/d and d/a conversion, output amplifiers, internal reference circuitry, and microprocessor interface. Though optimized for servo-control in hard-disk drives, it can be used generally in closed loop position-control. Included are a 4-channel 8-bit ADC (sharing two track-holds) and three d/a converters (two 8-bit and one 11-bit). Inputs can be sampled either independently or in simultaneous pairs.

External voltages independently set three key parameters: the

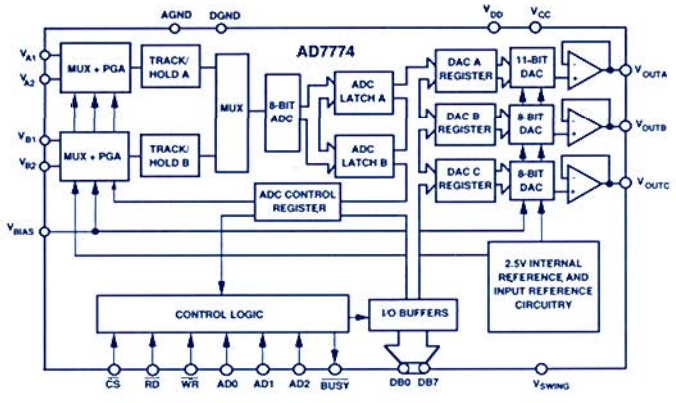
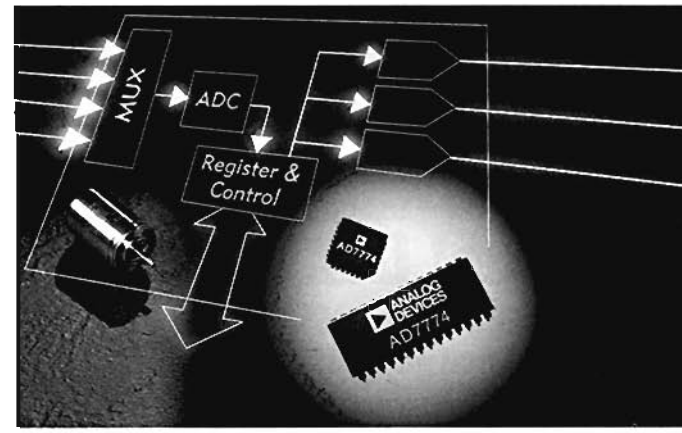


Figure 4: AD7774 Block diagram.



midpoint of the ADC transfer function (offset, or *bias* in disk-drive parlance), the input voltage swing of the ADCs (span), and the midpoint output voltage of the DACs (offset). Adjusting the offset and span matches the converters to the application; for example, the input and output voltages may be referenced to a point other than analog ground in single-supply applications.

Disk-drive applications: In disk drives with a dedicated servo track (Figure 5), the servo demodulator produces two positive voltages (*N* and *Q*, for *normal* and *quadrature*), with amplitudes of ($V_{BIAS} \pm V_{SPAN}$), from the data patterns read from the surface. Using the AD7774's simultaneous sampling, they are converted —without introducing significant phase delay errors—to provide the servo microcontroller with position- and track-crossing information, from which velocity can be derived.

The four channels of the AD7774 can be used for processing signals from two demodulators, or two channels can be used for a single demodulator while the other a/d conversion channels are used for measuring current, temperature, calibration, etc.

To position the head assembly in drives, a voice coil motor is generally used. One d/a converter, with resolution of up to 11 bits, is usually sufficient for both modes: *seek* (going to a new track) and *track* (following an acquired track position). In the AD7774, the high-resolution DAC is used for the voice coil while the lower-resolution DACs are used for programmable control of the loop filter—or other functions calling for programmable gain.

The AD7774 operates from +5-V and +12-V supplies. Fabricated in LC^2MOS, which combines precision bipolar circuitry with low-power CMOS logic, it is available in a 28-pin DIP and 28-terminal PLCC. Price is well below $18 in large volumes.

The AD897 was designed by Wyn Palmer and Janos Kovacs at Analog Devices in Wilmington, MA. The AD7774 was designed by a design team consisting of Philip Quinlan (Lead Designer), Hooman Reyhani, and Hiro Yamaguchi, with chip layout by Edel McMahon and Stuart Meakins, at Analog Devices' facility in Limerick, Ireland. ▶

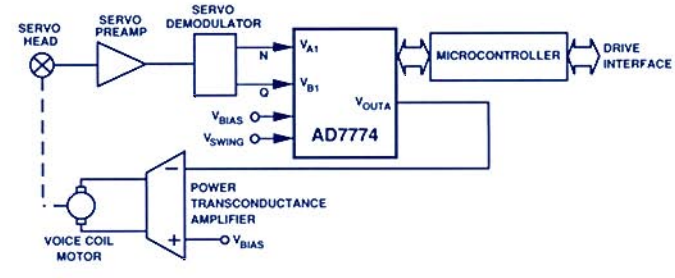


Figure 5: Typical dedicated servo loop.

3 New S/H Chips for Fast, Accurate Data Acquisition, and 8-Channel Distribution

AD9100 has a 30-MSPS encode rate; the AD682 dual guarantees 12-bit dynamic performance; SMP-18 multiplexes 8 channels

by Peter Predella

Analog Devices has introduced three important new sample/track-and-hold (S/H and T/H) amplifiers. Two are well-equipped for the demanding task of capturing signals that vary too quickly to be properly digitized by an a/d converter alone, and the third serves in multi-channel data distribution. Applications include r-f sampling, direct digital synthesis, ATE, and data acquisition.

Why a track/hold (T/H)? There are many reasons: an ADC may need it to catch a rapidly varying signal and maintain a constant input value during conversion, or to establish precisely the time associated with the converted data, or to obtain a train of regularly spaced data points for digital-signal-processing. In d/a conversion, a sample-hold is used to minimize glitches and as an accessory to non-double-buffered DACs for handling rapidly varying data; also, multiple sample-holds may be a low-cost alternative to multiple DACs for distributing data from the output port of a digital system to two or more analog channels.

If a signal changes by more than one-half of a least-significant bit (LSB) during a conversion, the converted value may no longer accurately represent the input existing at the time the conversion command was received. Performance can be improved by using a faster converter or one having an internal track-hold,* or—with a given converter—using an external T/H to acquire the signal and hold it during the conversion. The maximum sine-wave frequency (f_{max}) that can be converted with n-bit resolution without introducing more than 1/2-LSB error is related to the conversion-time uncertainty (T) thus:

$$f_{max} = 2^{-(n+1)} / T\pi$$

For example, a 12-bit converter that completes a conversion in 1 μs may have significant error at frequencies above *39 Hz*! If a track-hold with an aperture uncertainty of 1 ns (and an acquisition time in microseconds) is introduced ahead of this converter, the maximum frequency will increase to 39 *kHz*.

Dynamic performance: In high-speed applications, dynamic errors in converting high-frequency sine-wave signals are associated with noise and distortion—and reduced signal-to-noise ratio [SNR, sometimes known as S/(N+D)]. Since distortion of sine-wave (or sum-of-sine-wave) signals adds Fourier components, the spectrum of a distorted converted signal contains spurious peaks signifying harmonics, aliases of the higher harmonics (as well as intermodulation sum-and-difference products and their aliases) —and random noise (including components caused by aperture jitter). A properly designed- and employed T/H amplifier will greatly reduce both spurious signals due to distortion and random noise caused by the original jitter.

*Examples of sampling a/d converters include the AD773, AD1876, and AD7886, introduced in this issue, or the AD1674, introduced in issue 25-1.

†Use the reply card for data. Circle 8

VIDEO SPEED, 12-BIT PERFORMANCE

The AD9100† is the industry's fastest T/H amplifier with true 12-bit performance. At 30 megasamples per second (MSPS), its timing characteristics and dynamic performance are unmatched (see Table 1). Using a new (patented) closed-loop architecture built on a high-speed complementary-bipolar (CB) IC process, the AD9100 offers low distortion, yet maintains the slew rate specs of traditional open-loop designs. Maximum acquisition time of a 2-V signal to within 0.01% is 23 ns (16 ns typical). With an encode rate of 30 MSPS, hold-mode distortion is specified for input frequencies up to 20 MHz (Figure 1).

Table 1. Comparative Key Specifications

Model:	AD9100	AD682	SMP-18	Units
Sample Rate	>30	0.5	0.2	MSPS
Track Mode Dynamics				
Bandwidth (–3 dB)	250 (160 min)	4 (1-FP)		MHz
Slew Rate	850 (550 min)		6	V/μs
Hold Settling Time	0.011	0.5	1	μs, max
Aperture Delay	+800	–25 ± 10		ps
Aperture Jitter	<1	75 max		ps
Acquisition Time				
to 0.01% (2 V step)	16 (23 max)			ns
to 0.1% (6 V step)			2.5	μs
to 0.01% (10 V step)		0.7		μs, max
Droop Rate	1 (6 max)/μs	1/ms max	2 (40 max)/s	mV/(t)
Hold offset	±1 (±5 max)	–1 (+3, –4 max)	4 (6 max)	mV
Output Drive	±60 (±40 min)	±5	10	mA
Power Dissipation	1.25 max	0.32 max	0.05	W
Pricing, 100s	$69	$12	$6.95	US

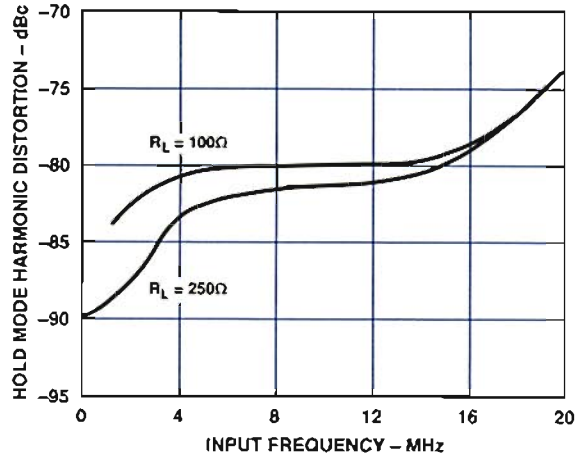


Figure 1. AD9100's Hold-mode distortion as a function of frequency.

The AD9100 can extend the dynamic range of 8- and 10-bit flash converters, as well as higher-resolution moderate-speed data-acquisition converters, to encode signals at up to 30 MSPS. Its applications include direct RF/IF sampling, imaging systems, peak detection, spectral analysis, and buffering of high-speed converter inputs. The encode clock drive for its patented switching circuitry is differential-input ECL; jitter is less than 1 picosecond. The analog inputs are internally clamped to prevent damage from voltage transients.

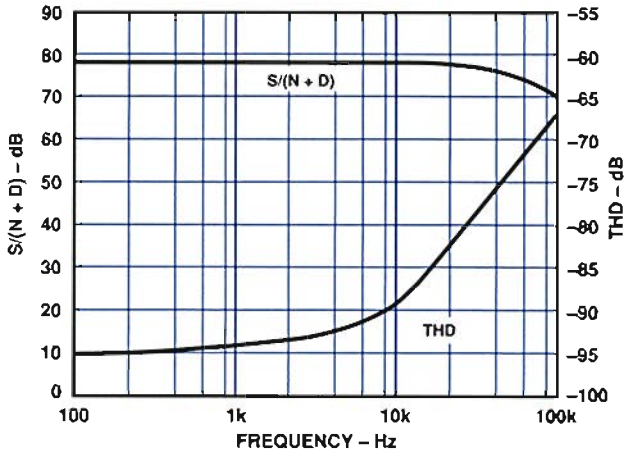


Figure 2. AD682's signal-to-noise performance.

Packaged in a 20-pin ceramic DIP and powered from +5-V and –5.2-V supplies, the AD9100 includes a hold capacitor and decoupling capacitors for the switch's power supply. Grades are available specified for the commercial (0 to +70°C), industrial (–25°C to +85°C), and military (–55 to +125°C) temperature ranges. An LCC package is available for surface-mount users.

DUAL S/H WITH 12-BIT DYNAMIC SPECS

If your next high-speed multichannel application requires two channels of sample/hold with 12-bit dynamic performance, the AD682§ is a highly cost-effective choice. At a 500-ksps sampling rate, guaranteed maximum THD (see Figure 2) and minimum signal-to-noise plus distortion (S/N + D) at input frequencies up to 10 kHz are –80 dB and 72 dB, respectively. For higher frequencies—50 kHz and 100 kHz—the respective THD values are –73 and –68 dB, and for SNR, 73 dB and 67 dB. The AD682's 2nd- and 3rd-order IMD products are –77 and –78 dB.

Like its single- and quad-channel versions (AD781 and AD684), the AD682's combination of frequency- and time-domain (ac and dc) specs make it a first choice for traditional data-acquisition applications as well as sampled-data systems. Consider for example its acquisition time and hold-mode performance: full-scale steps of 10-V can be acquired to within 0.1% (10 bits) in less than 600 ns and to 0.01% (12 bits) in less than 700 ns; aperture delay and jitter are –25 ± 10 ns and 75 ps max; and hold settling time to 1 mV is just 500 ns. Isolation between channels is 90 dB max; and worst-case interchannel mismatch specs are 1.5-mV for voltage offset and 300 ps for aperture time.

Both channels include on-chip capacitors and are configured for unity gain. The AD682 operates from ±12-V supplies and has an input range of ±5-volts. Both commercial (J-grade) and industrial (A-grade) devices are available packaged in a 14-pin DIP. MIL-temp range (S-grade) devices, specified from –55°C to +125°C, are packaged in 14-pin cerdips.

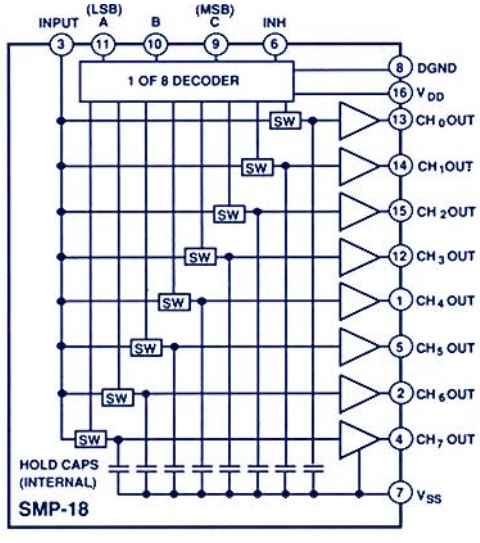


Figure 3. Block diagram of the 8-channel SMP-18.

DRIVING MULTIPLE ANALOG CHANNELS

The SMP-18‡, a new octuple S/H amplifier combines an input multiplexer and eight output buffer amplifiers, each with its own hold capacitor, in a single 16-pin DIP or SOIC (Figure 3). When used with an 8-bit, 10-volt-full-scale d/a converter, its 10-mV max buffer offset (20 mV over temperature) is less than 1/2 LSB. The SMP-18 has low nonlinearity (0.01% typical), fast acquisition time (2.5 μs), low droop rate (40 mV/s max, 2 typ), low dissipation, and high immunity to latch-up. Pin-compatible with the SMP-08 (*Analog Dialogue* 24-3), the SMP-18 provides the same function with nearly tripled speed. Working with a low-cost 8- or 10-bit d/a converter, the SMP-18 readily brings multichannel output to microprocessor-based systems.

In multichannel applications, including per-pin IC automatic test systems (Figure 4), the SMP-18 is useful for level-setting and scaling circuitry, calibration and de-skew networks, and for manipulating system parameters. Other applications, including multipoint data-acquisition systems and general-purpose memory programmers, can benefit from the SMP-18's compactness. Compared to discrete designs and devices with lesser degrees of integration, the SMP-18 significantly reduces size and cost.

The SMP-18 is TTL/CMOS compatible and operates from either a single +12-V supply or bipolar ±5-V supplies. No external logic components are required for direct interfacing to DACs, since break-before-make switching and decoder logic are included on-chip. The SMP-18 is specified for operation over the extended industrial temperature range, –40 to +85°C.

The AD9100 was designed by Roy Gosser at ADI's Computer Labs Division in Greensboro, NC; the AD682 was designed by Chris O'Connor at our Wilmington, MA Semiconductor Division; The SMP-18 was designed by Paul Collanton at the PMI Division in Santa Clara, CA.

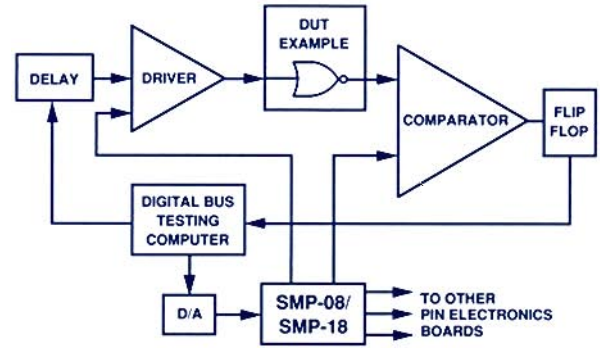


Figure 4. Typical multi-channel-output application of the SMP-18 in ATE.

§Use the reply card for technical data. Circle 9

‡Use the reply card for technical data on the SMP-18 or Application Note AN-204 on the SMP-04/08/18. Circle 10 for data, 11 for app. note

Monolithic 10-Bit, 18 MSPS Sampling A/D Converter with on-Chip Track-Hold

AD773 has a 100-MHz signal bandwidth, –66-dB THD at 1 MHz, only 1.2-W dissipation; is lowest-cost 10-bit video ADC

The AD773* is a monolithic sampling analog-to-digital converter with 10-bit resolution. Combining an input track-and-hold amplifier (THA) and a digitally corrected subranging a/d converter, it is capable of converting video-bandwidth signals, sampling at rates up to 18 megasamples per second (MSPS). The THA's wide frequency range (typically 100 MHz, full-power) is ideal for wide-band input signals and in undersampled applications.

For high performance and ease of use, the track-and-hold analog input has high input impedance and a choice of differential- or single-ended operation (Figure 1). This eliminates external buffers and sample-holds, saving power and board space. The reference input is also at high impedance; it will operate with standard 2.5-volt references such as the AD680, AD580, and REF-43. The AD773's dissipation, 1.5 W max (1.2 typical), is among the lowest for 10-bit video a/d converters; and—packaged in a convenient 28-pin ceramic DIP—its price is *the* lowest: $55 in 100s (AD773JD).

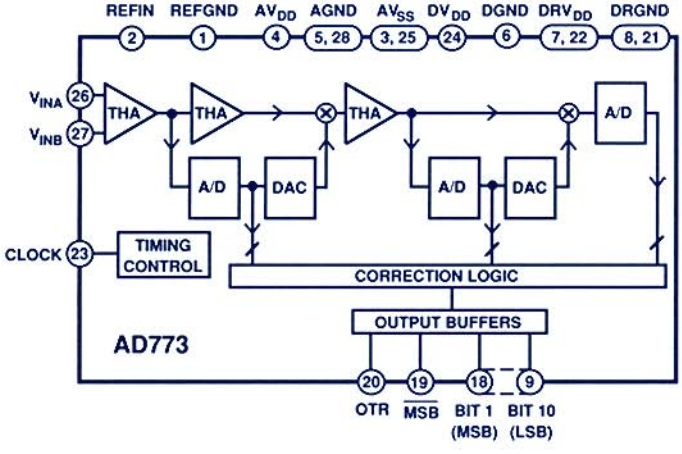
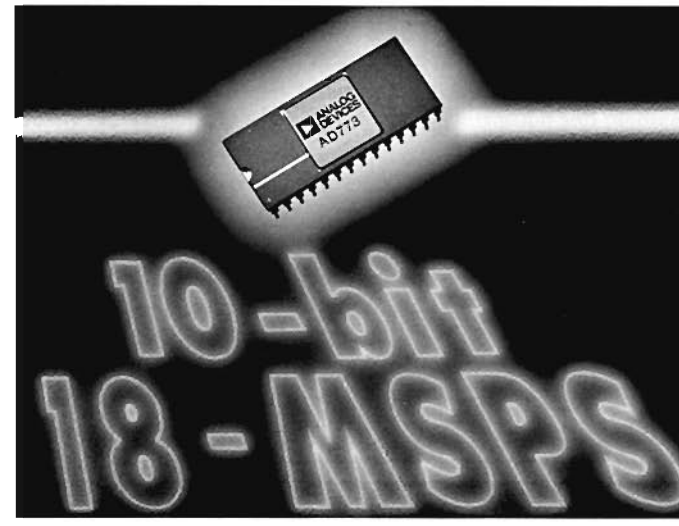


Figure 1. Block diagram

Applications abound in a gamut of fields. Examples include: high-performance composite and component video—including post-production equipment, video tape recorders, and HDTV; imaging systems—including ultrasound, infrared, and radar; as well as communications and high-speed instrumentation.

The AD773 employs three 4-bit flash a/d converters in a three-stage pipelined architecture, with digital correction logic. This multistage architecture reduces power dissipation and die size—compared to full flash conversion—by greatly reducing the number of comparators. Output data is available in a choice of binary or twos-complement form. The AD773 will flag an out-of-range signal when the analog input exceeds the full-scale range (nominally 1 V p-p) by 1/2 LSB; though generally useful, this feature is especially desirable in recursively controlled programmable-gain signal conditioning.

*Use the reply card for technical data. Circle 12



Dynamic performance of the AD773K, sampled at 18 MSPS with 1 and 8.1-MHz sine-wave inputs, includes signal to noise-plus-distortion [S/(N+D)] of 56 dB and 53 dB (typical). Total harmonic distortion for 1 and 8.1-MHz sine waves is typically –66 and –58 dB. Spurious-free dynamic range (SFDR) for 1-MHz input is typically 67 dB, and 2nd and 3rd-order intermodulation products (1.0 and 1.05 MHz inputs) are typically –69 and –61 dB. Figure 2 is a typical FFT response plot. Full-power bandwidth is typically 100 MHz, with settling time of less than one clock cycle for a full-scale swing. Differential phase and gain are 0.2° and 0.4%. Linearity is good over the temperature range: ±2-LSB max integral nonlinearity and ±1 LSB max differential nonlinearity, with no missing codes guaranteed.

Nominal power supply voltages are ±5 V; and the AD773 is TTL/CMOS-compatible. Grades now available are J and K, for 0 to +70°C; military temperature-range versions will also be available. For an evaluation board, call your local sales office.

The AD773 design team was led by Peter Real and Dave Robertson at Analog Devices Semiconductor Division's Converter Group, Wilmington, MA.

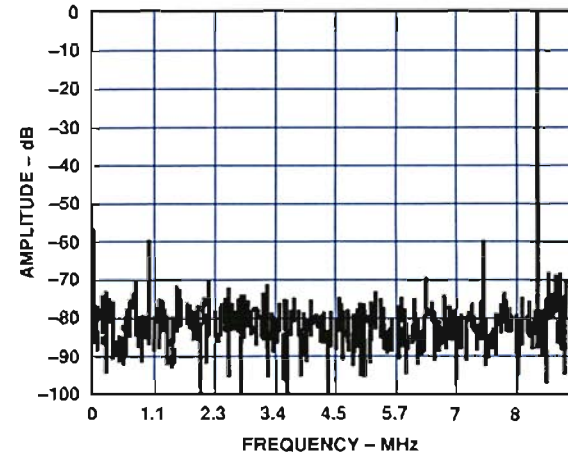


Figure 2. FFT plot of output for 18-MSPS clock and 8.5-MHz input signal. –60-dB "spikes" are aliases of 2nd and 3rd harmonics.

Complete 16-Bit DACPORT in SOIC Package Includes on-Chip 10-V Reference

Low-cost AD669's output span is programmable. 16-bit double-buffered latches eliminate glue logic and simplify μP interface

by Peter Predella

The AD669* DACPORT™, a complete monolithic 16-bit digital-to-analog converter (DAC), includes a buried-Zener reference, span-programmable output amplifier and double-buffered latches. With it, a 16-bit computer bus can be interfaced to the analog world with a minimum of external circuitry. Applications for the DACPORT include multipoint industrial and laboratory automation and control systems, precision analog signal generation systems, and simultaneous sampling instrumentation. The AD669 can also simplify the upgrade path from 12- and 14-bit interfaces, reducing system design effort and costs.

Guaranteed and tested ac and dc characteristics include monotonicity over temperature to 15 bits, maximum ±1-LSB integral and differential nonlinearity (B grade), maximum 0.009% THD+N (full scale) and 84-dB SNR. Other key performance specifications include a 30-ns data setup access time and 40-ns write time (to handle a wide range of processors), 15-nVs glitch energy (impulse). For a full-scale input step and a bipolar output swing, the output settles to within ±0.0008% in just 13 μs, with 2-kΩ output load.

When required by the system, data is loaded into the AD669's first rank of latches in a standard parallel 16-bit format; then the data can be asynchronously transferred to the DAC latches whenever the analog data needs to be updated The double-buffered latches eliminate data skew errors and facilitate multichannel and

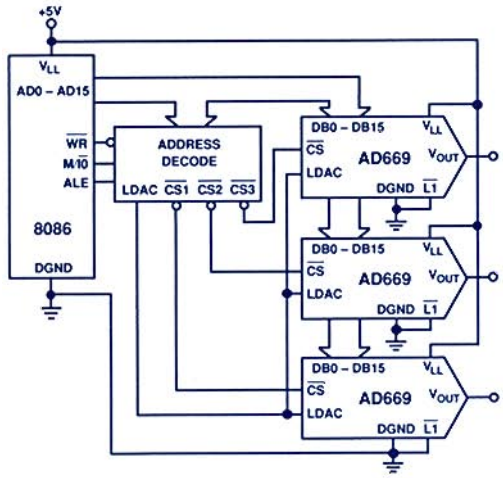
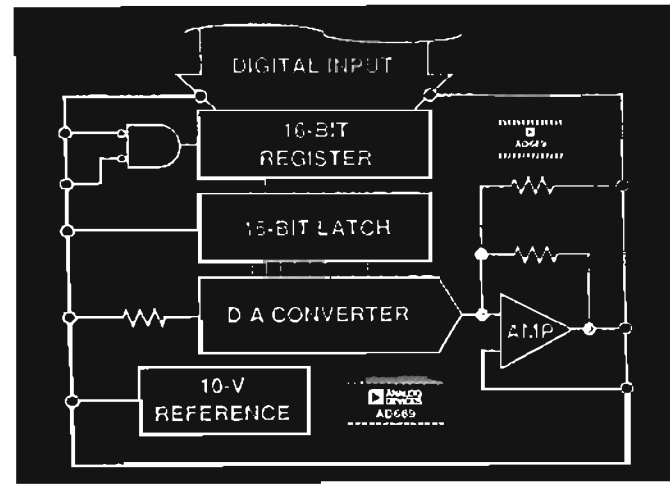


Figure 1. Interfacing the AD669 to an 8086 16-bit microprocessor in a multi-DAC environment—logic connections.

*Use the reply card for data. Circle 13



simultaneous sampling applications without the need for external glue logic to microprocessors. Just three control signals compatible with TTL, LSTTL, or 5-V CMOS are needed to control the latches. Figure 1 shows a scheme for interfacing several DACs to an 8086 16-bit microprocessor. The μP can write to each AD669 individually; and all outputs can be updated simultaneously. Processors with speeds up to 10 MHz can be interfaced without wait states.

An internal low-noise buried-Zener-diode circuit provides a stable reference, trimmed for absolute accuracy to within 0.2%. Buffered to drive external circuitry, it can act as a system reference, providing at least 2 mA (and more with external buffering).

The d/a converter portion uses an array of bipolar current sources with MOS current-steering switches to develop a current between 0 and 2 mA, proportional to the applied digital word. The four MSBs are decoded to sum up to 15 equal (1/16-full-scale) current sources; the other 12 bits are scaled with an R-2R ladder, then summed with the MSBs at the buffer amplifier's summing node.

The output amplifier is pin-programmable for unipolar or bipolar span. An on-chip resistor can be externally wired to either the DAC's output for a span of 0 to +10 V, or to the reference input to provide a full-scale −10 V to +10 V range.

Packaging options include 28-pin SOICs (the industry's smallest footprint available among 16-bit DACs), cerdips, and plastic DIPs. Operating temperatures range from −40 to +85°C, and −55 to +125°C. '883 versions will be available. Prices start at $16 (100s).

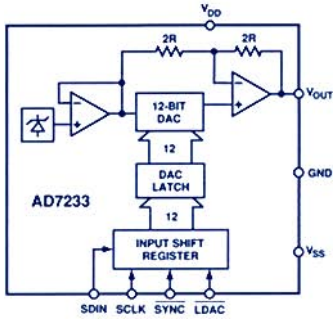
The AD669 was designed by Michael Coln at Analog Devices Semiconductor, Wilmington, MA.

Table 1. AD669 Key Specifications

Grades:	AN/AR	AQ/SQ	BN/BQ/BR	Units
Resolution	16	16	16	Bits, min
INL	±2	±2	±1	LSB, max
DNL	±2	±2	±1	LSB, max
Gain error	±0.15	±0.1	±0.1	% FSR, max
Reference error	±0.2	±0.2	±0.2	%, max
Unipolar offset	±5	±5	±2.5	mV, max
Bipolar zero error	±15	±15	±10	mV, max
Output settling time	13	13	13	μs, max
THD + N	0.009	0.009	0.009	%, max
Signal-to-noise	84	84	84	dB, min
Power Dissipation	365	365	365	mW

SERIAL DACS

In 12-Bit DIPs & SOICs: AD7233/43 DACPORTs



The AD7233/AD7243*, industry's smallest complete serial-input 12-bit DACs, are 12-bit DACPORTs™—complete, ready-to-interface single-chip voltage-output d/a converters. Using a simple 3-wire interface to most DSP processors and microcontrollers, they can be clocked at up to 5 MHz, for a 300-kHz update rate. Full accuracy is maintained to beyond 100 kHz, since the DACs' maximum full-scale settling time is 10 μs to ±1/2 LSB.

Both devices, fabricated in ADI's linear-compatible CMOS (LC^2MOS) process, include on-chip buried Zener references and output amplifiers—and have similar performance specs. They differ in pinout, input format, output range, reference connections, controls, and package choices.

Over temperature, both devices have ±0.9-LSB max differential nonlinearity ±1/2-LSB max relative accuracy error (B grade), and are guaranteed monotonic. They dissipate 100 mW. Prices (100s) start at $7 for both.

AD7233 accepts digital twos-complement input, has an internally referenced −5 V to + 5 V output, and is packaged in an 8-pin mini-DIP. It is available in A and B grades for the −40 to +85°C temperature range.

AD7243 is available in 16-pin plastic DIP, cerdip, and small-outline (SOIC) packaging. Its output is pin-programmable for unipolar (0 to +5 or +10 V) or bipolar (−5 to +5 V: offset binary or twos complement). A CLR input resets the output to zero on command. The reference is jumpered externally, so the AD7243 can can either accept or serve as a reference for external circuitry.

*DACPORT is a trade mark of Analog Devices, Inc.
Use the reply card for information. Circle 14

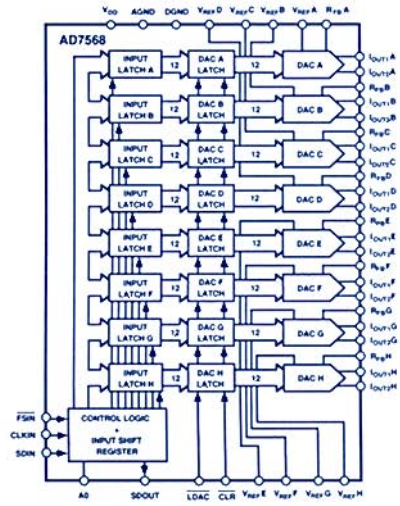
EIGHT 12-BIT M-DACS ON A CHIP

Serial-input monolithic AD7568: first-in-industry, single +5-V supply, separate reference inputs

The serial-input AD7568† contains an octet of 12-bit current-output 4-quadrant multiplying d/a converters on a monolithic CMOS chip, housed in a 44-pin PQFP. It is powered by a single +5-volt supply and dissipates only 1 mW. Each independently addressable DAC has its reference terminal and feedback-resistor—and both of its current outputs—available for connection; thus each DAC can be configured and operated independently; yet all DACs can be simultaneously updated or reset to zero.

The AD7568 is useful for fixed- and variable-reference applications requiring more than four 12-bit DACs with a common serial digital source. Examples include multipoint automatic testing, process-control systems, audio mixing, battery-powered remote instrumentation

Guaranteed monotonic over temperature, it combines excellent linearity (±1/2-LSB max relative-accuracy error, ±0.9-LSB max



differential nonlinearity) and fast settling (500 ns to 0.01% FSR with the AD843 as output amplifier). It is available in a top-grade "B" version (−40 to +85°C). Price is $28 in 100s—about $3.50 per channel.

†Use the reply card for technical data. Circle 15

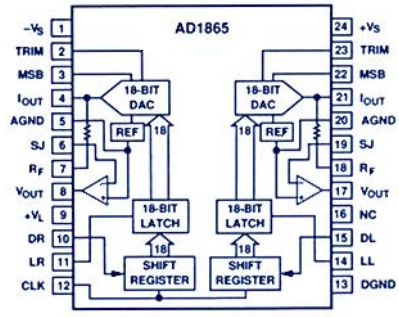
DUAL 18-BIT AUDIO DAC

AD1865 has 107-dB min SNR, 16× oversampling Improved performance over AD1864, same price

The AD1865† is a monolithic dual-18-bit serial-input, voltage-output DAC for digital audio. Complete on a single chip and housed in a 24-pin plastic DIP or 28-pin SOIC package, its two conversion channels include pairs of references, DACs, latches, amplifiers, and scaling resistors; no external components are required.

Salient specifications include: signal-to-noise—SNR (from 20 Hz to 30 kHz) 107 dB min; total harmonic distortion plus noise—THD+N (at 0 dB, 990.5 Hz) 0.006% max; 110-dB minimum channel separation; 0.3% typical interchannel gain matching; 1% max gain error; and 88-dB min D-range. A premium "J"-version, with 0.004% max THD+N, is also available.

Applications include such consumer digital audio entities as compact-disc players, digital audiotape players and recorders, and automotive audio systems; multivoice keyboard instruments and other electronic musical in-



struments; digital mixing consoles for professional studio, recording, and broadcast equipment; and multimedia workstations.

The availability of two complete signal channels on-chip results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The AD1865 is physically and electrically compatible with, but features improved performance over the earlier AD1864, at the same price. Prices start at $20.45 in 100s.

†Use the reply card for technical data. Circle 16

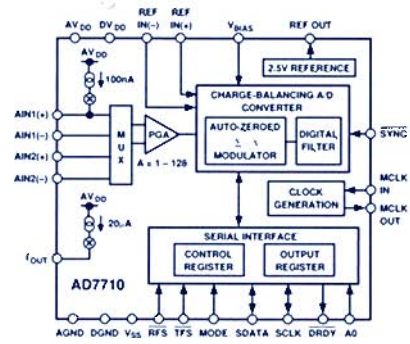
SINGLE-CHIP DATA ACQUISITION

AD771X Σ–Δ family has PGA, 21-bit A/Ds, Direct transducer interface, digital filter

Designed as complete analog front ends for low-frequency measurement applications with transducers—such as strain gages, RTDs, and thermocouples—the AD771X* family of small, low-cost, monolithic data-acquisition chips performs a/d conversions with 21-bit resolution. Nonlinearity is ±0.0015% maximum with no missing codes; each device includes a software-programmable-gain amplifier (PGA) with a gain range from 1 to 128 V/V. Interfacing is via a bidirectional serial port.

The PGA and Σ–Δ architecture reduce the need for preamplifiers or front-end signal conditioning. In addition, the device has excellent 50/60-Hz rejection (100 dB min), digital low-pass filtering (software-programmable cutoff frequency), and both internal- and user-writeable self-calibration.

The **AD7710*** is designed for low-level signal sources, e.g., strain gages. It has two differential inputs plus a differential reference input that can be used for calibration.



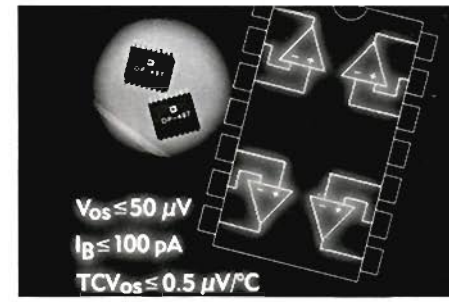
For RTDs, the **AD7711†** provides two 200-μA current sources for excitation, a differential input, and a differential reference input. For handling signals with a wider range of input voltage, the **AD7712§** provides attenuation as well as gain.

Dissipation is 25 mW (50-μW power-down); packaging is in 0.3" DIPs and 24-lead SOICs. Prices (AD7712 in 1000s) start at $11.90

*†§Use the reply card for technical data.
Circle 17 (AD7110), 18 (AD7111), 19 (AD7112)

QUAD OP AMP

OP-497 has industry's highest precision



The OP-497¶ comprises four op amps combining high open-loop gain, low offset voltage and drift, and low bias current. It is a quad version of the dual OP-297 and single OP-97, well suited for designs needing a number of precision amplifiers, small space, and low power consumption. Typical applications include instrumentation-amplifier designs, photodiode preamplifiers, and amplifiers for thermocouples and strain gages.

Guaranteed specifications include 50 μV maximum offset voltage at 25°C, drift of 0.5 μV/°C, maximum bias current of 100 pA at 25°C—rising to only 450 pA at 125°C, 2×10^6 open-loop gain, and 625 μA maximum supply current per channel.

Low offset voltage and high gain eliminate offset trims and additional gain stages in many designs. Battery-powered systems benefit from the OP-497's low supply current, ability to operate from any supply voltage between ±2 V and ±20 V, and 120-dB power-supply rejection. CMR is guaranteed at 120 dB min, with a common-mode range to within 1 V of the supply rails.

The OP-497's superbeta input stages with bias-current cancellation circuitry maintain subnanoampere bias current over the full operating temperature range. This contrasts with FET-input amplifiers; their initially low bias current doubles with each 10°C increase in temperature. Low I_{bias} is useful in low-leakage, wide-temperature-range applications such as sample-holds, peak detectors, and log amplifiers.

The OP-497 is available for −40 to +85°C and −55 to +125°C, and in SOIC, LCC, and 14-pin plastic and cerdip packages. Prices start at $4.75 (100s).

¶Use the reply card for technical data. Circle 21

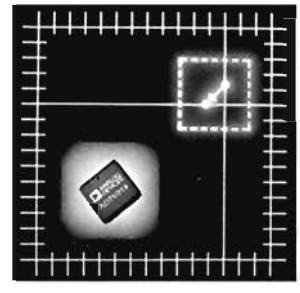
16 × 16 ANALOG IC SWITCH ARRAY

AD75019 crosspoint switch handles up to 24 V p-p Cell-based design allows custom extensions

The AD75019‡, a bidirectional CMOS analog switch housed in a 44-contact PLCC, connects up to 16 inputs to any or all of 16 outputs (256 points). TTL/CMOS-compatible address data is clocked serially—from 20 kHz to 5 MHz—into a 256-bit shift register, then to 256 on-chip latches. Applications exist in test, medical, audio, etc.

With a supply-voltage span of from 9 V to 24 V (unipolar or split as required), the AD75019 is specified at ±12 V and ±5 V; it will handle signal voltages up to the supply rails. With ±12-volt supplies, it draws a maximum quiescent current of ±400 μA; with ±12-V signals, max On resistance is 300 Ω (150 typical). Leakage current is 2 nA, 10 max (±10-V signals); and inter-channel isolation is 92 dB min for 2-V p-p signals at 1 kHz. Its price is $15 in 100s.

The number of switches can be increased by cascading AD75019s, connecting SOUT of

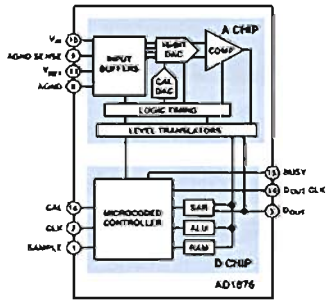


one device to SIN of the next. Moreover, the array is a customizable *linear system macro* (LSM); its cells are all from Analog Devices' BiMOS II standard-cell library. The basic architecture can be adapted using other library cells at much less cost than that to design a custom ASIC. For example, we might add input or output signal buffers or provide a parallel control interface. For information about customized ICs in quantity, call an Analog Devices Sales Engineer.

‡For technical data, use the reply card. Circle 20

SAMPLING ADC

16-bit, 100-ksps, serial, autocalibrated AD1876



The AD1876* is a 16-bit serial-output sampling a/d converter capable of sampling at rates from 1 to 100 ksps (total conversion time 10 µs, aperture jitter 100-pVs). Designed with a switched-capacitor/charge-redistribution architecture, embodied in 2 chips employing compound monolithic integration (CMI), it is housed in a 0.3" ("skinny") 16-pin plastic DIP. Price is only $25 (1000s).

The AD1876 has an input voltage reference range of from 3 to more than 7 volts and a full-power bandwidth of 1 MHz. Dynamic specifications include S/(N+D) of 83-dB minimum, 87 typical (48-kHz bandwidth), total harmonic distortion of –88 dB max (0.004%), –95 dB (0.002%) typical. Other ac specs include –89 dB max (–99 dB typical) peak spurious or peak harmonics, 92-dB D-range (–60 dB, A-weighted).

AC performance is also specified for –20-dB and –60-dB input levels. Typical intermodulation products are –102 dB second-order and –98 dB third order.

Overall performance is optimized by digital correction of internal nonlinearities through on-chip autocalibration. The output format is serial twos complement, directly compatible with the NPC SM5805 digital decimation filter used in consumer audio products. Typical applications include signal processing, audio, and general instrumentation for ac signals. Other products employing this technology will soon be available with excellent ac *and dc* specs.

Supply requirements are ±12 V and +5 V, with 235-mW typical power consumption; its specified temperature range is 0 to 70°C.

*Use the reply card for technical data. Circle 22

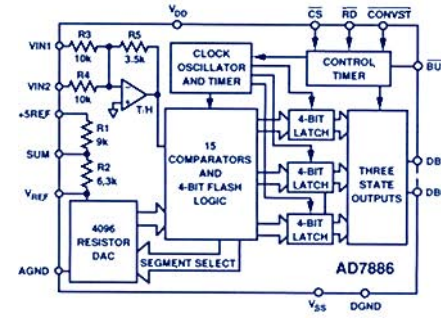
12-BIT, 750-KSPS SAMPLING ADC

Monolithic AD7886 dissipates only 350 mW max, interfaces directly with all standard DSPs

The AD7886† monolithic 12-bit sampling a/d converter is capable of throughput rates up to 750 kHz. Specifying no missing codes over temperature with 12-bit resolution, it has a low power-dissipation—typically 250 mW. Its data access time of less than 57 ns means that the AD7886 can interface directly to most modern microprocessors, including DSPs.

While broadly applicable in data acquisition, the AD7886 is especially useful for sampling and converting both high-frequency signals and multiplexed lower-frequency signals. Typical application areas include digital signal processing, speech recognition and synthesis, spectrum analysis, and DSP servo control.

Its signal-to-noise ratio (including distortion), is 67 dB min (K, B grades), with typical THD and peak spurs of –75 and –77 dB, respectively, for a 100-kHz sine wave input sampled at 750 kHz. Integral nonlinearity is ±2 LSB max over temperature (K, B, T).



The AD7886, fabricated in linear-compatible CMOS (LC^2MOS) is available in grades for 0 to 70°C, –40 to +85°C, and –55 to ±125°C. It requires ±5-volt supplies and a –3.5-V reference. Pin-programmable input voltage ranges are 0 to +5 V, 0 to +10 V, and ±5 V. The digital data interface is a 12-bit parallel word. 28-pin ceramic DIP and PLCC packaging are available. Prices start at $55 (AD7886JD/JJ in 100s).

†Use the reply card for technical data. Circle 23

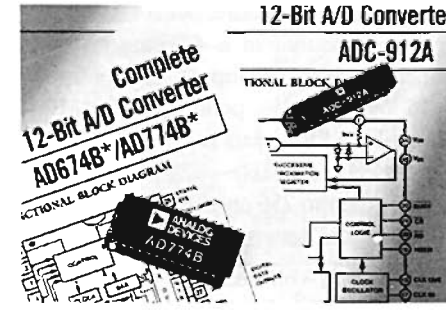
FLEXIBLE 12-BIT, 8-10-µs ADCS

AD774B: improved performance for '574 sockets

ADC-912A: low cost, low power, small package

The AD774B‡ and ADC-912A§ are two new high-performance (1/2-LSB integral nonlinearity) monolithic successive-approximation 12-bit a/d converters that interface to 8- or 16-bit buses. Each meets a set of specific needs.

The **AD774B‡** is a fast (8-µs) ADC, complete with a 10-volt internal buried-Zener reference and 0-10 V, 0-20 V, ±5 V, and ±10 V pin-programmable input ranges. Packaged in 28-lead plastic or ceramic DIPs (and soon SOICs), it is a fully compatible speed upgrade for industry-standard 574/674 converter sockets—with improved noise immunity over the AD674A. Using +5-V and ±15- or ±12-V supplies, it is available for 0 to 70°C, –40 to +85°C, and –55 to +125°C temperature ranges. Prices start at $25.70 in 100s, $19.15 in 1000s (AD774BJN).



The **ADC-912A**, with a 10-µs conversion time and featuring low transition noise, is a CMOS chip housed in compact 24-pin 0.3" "skinny" plastic and cerdip, or 24-pin low-profile SOIC packages. Using +5 and –12-V supplies, it dissipates only 95 mW and is available for the –40 to +85°C temperature range. It requires an external –5-V reference and has a 0 to +10-V input range. Prices start at $12 in 100s, $10 in 1000s.

‡Use the reply card for technical data. Circle 24

§Use the reply card for technical data. Circle 25

Advanced SPICE Op-Amp Macromodel: A Powerful Tool for Designers

by Joe Buxton

SPICE simulation can speed the development time-to-market of analog system designs. The increasing use of SPICE for this purpose has led to an increase in demand for accurate macromodels of linear ICs. Until recently, most SPICE software packages came with an extensive library of discrete transistors, but only a very limited number of such linear ICs as operational amplifiers; this forced designers to fend for themselves in simulating their systems. Analog Devices responded to this need with an effort to develop an advanced op amp macromodel. The resulting Analog Devices SPICE model[1]* ["ADSpice" model] has excellent ac and transient response characteristics, complete dc characteristics, and full noise-analysis capabilities.

ADSPICE DEVELOPMENT GOALS

The development effort was undertaken with specific goals in mind. At the time, the existing state-of-the-art op-amp model was the "Boyle" model[2]. While adequate for lower-speed amplifiers, this model lacked adequate capabilities to simulate the complex gain and phase response of many of today's higher-speed op amps. Thus, our primary goal was to develop a model that, by incorporating an unlimited number of response-shaping poles and zeros, would result in more-accurate ac and transient simulations.

The ADSpice model was also designed to model accurately most of an op amp's dc parameters. A notable improvement over the Boyle model is the ability to model the supply current correctly as a function of both the device's quiescent current and the output current load. This is essential for engineers analyzing power dissipation or designing circuits that mirror the supply currents.

An additional recent goal is to provide noise-analysis capabilities. The basic model is rendered "noiseless," then independent sources of broadband (white) and $1/f$ noise are added.

Another important goal was to make the ADSpice model easy to develop and change. Designers frequently need to see how their circuit reacts to changing op amp parameters. By using an open architecture for the model, an engineer can easily change individual parameters. For example, the offset voltage can be changed by simply altering an independent voltage source.

THE AD SPICE MODEL STRUCTURE

The goal of making the model easy to develop and change resulted in a modular structure comprising individual stages. The stages are connected only through ideal SPICE voltage controlled sources, which allows the op amp parameters to be modelled and changed separately. For example, all the pole and zero stages have unity low-frequency gain. As a result, any number of them can be added to the model; but their influence is limited to the intended effect of changing the gain and phase response at higher frequencies.

*Use the reply card for a free ADSpice Library diskette. Circle 26

In creating the model the use of transistors and diodes was kept to a minimum. Instead, ideal SPICE elements—such as voltage-controlled current sources and simple resistors and capacitors — model an op amp's behavior. This keeps the simulation speed reasonable, and in addition avoids revealing proprietary circuit details. The ADSpice macromodel can run orders of magnitude faster than a full transistor-level micro-model.

The input stage and gain stage

Using the only two transistors in the model, the input stage shown in Figure 1 models most of the DC characteristics of the op amp. The most important characteristics are also the simplest to calculate and change. For example, a DC voltage source, V_{OS}, placed in series with the input, is set to the device's offset voltage. The element I_{OS}, set at one-half the offset current, adds equal and opposite input current increments to the transistor bias currents. As these two examples demonstrate, changes to most dc parameters require only a simple adjustment of a particular SPICE element. Replacing the NPN bipolar transistors shown here by PNP or JFET devices will not change the basic structure.

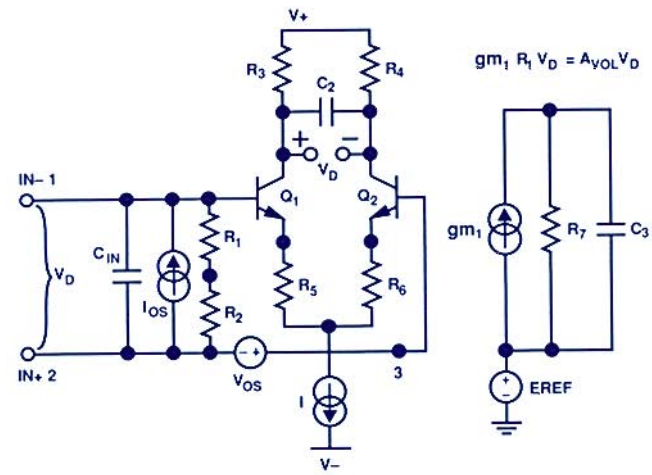


Figure 1. Input- and gain stages.

The gain stage, closely paired to the input stage, sets the open-loop gain, dominant pole, and slew rate. The voltage controlled voltage source, g_{m1}, senses the differential voltage, V_d, between the collectors of Q1 and Q2. The transconductance, g_{m1}, multiplied by R_7, sets the entire open loop gain of the amplifier. This implies that all other stages are normalized to unity gain, which, as explained below, is important for the AC accuracy.

Pole and zero stages

Immediately following the gain stage are a series of pole- and zero stages that shape the higher-frequency gain and phase response (Figure 2). Each stage independently sets a pole and/or zero frequency; because their gain is unity, one can add as many as are needed. This provides the flexibility required to model an op amp's frequency response accurately. The pole stage is very similar in structure to the gain stage. However, with g_{m2} set equal to the reciprocal of R_8, the stage will have unity gain. The pole frequency is then set by the capacitance, C_4.

The gain of the voltage-controlled voltage source, E_1, in the zero stage is made equal to the attenuation from the resistance divider formed by R_9 and R_{10}, providing overall unity gain. The attenuation ratio is set at 10^6 to 1, so that the zero's characteristic frequency, set by R_9 in parallel with C_5, is six decades lower than the pole formed with R_{10}, which becomes insignificant.

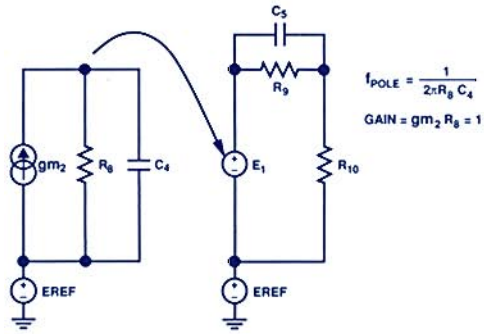


Figure 2. Pole- and zero stages.

Output stage

The output stage models the output impedance, short circuit current limit and the power supply current (Figure 3). In addition to modelling the output resistance, an inductor is also included in series with the output, to model the high-frequency rise in impedance. To ensure unity gain in the output stage, the values of g_{m5} and g_{m6} are set to the reciprocals of R_{11} and R_{12}. An important requirement of the output stage is the proper modelling of the supply current as a function of the output current. To ensure this, an absolute-value circuit for the current was added, comprising g_{m3}, D_7, D_9, and g_{m4}, D_8, D_{10}.

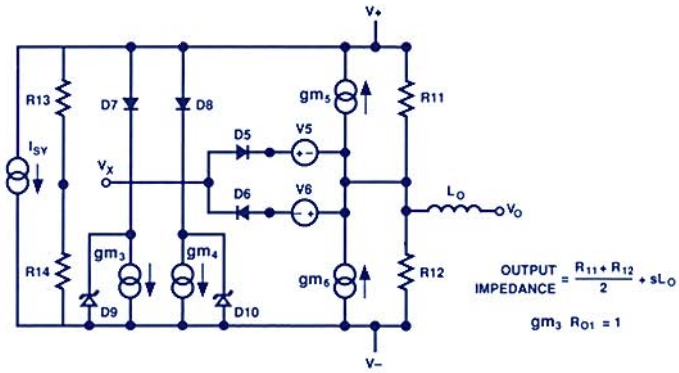


Figure 3. Output stage.

A more complete description of the model, including the equations to set the elements, is included in the application note AN-138[1]. For amplifiers not included in the Analog Devices SPICE model library (for example, the occasional device from another manufacturer), much of the ADSpice model can be calculated using AN-138 and an amplifier's data sheet. However, the specific pole and zero locations for a given part type are determined from detailed gain and phase responses. For best results, these are measured for actual parts using an instrument such as a network analyzer. Then the model's frequency response can be fit to the actual amplifier's curves. With these two tools (and some time), a complete model for a specific amplifier can be developed.

THE ADSPICE NOISE MODEL

Noise analysis is an important feature long missing from SPICE op amp macromodels. The benefits of simulating noise performance are immediately obvious to anyone who has attempted to do noise analysis by hand—a tedious job at best. It involves calculating the noise contribution of each individual resistor, transistor, and op amp, and then root-mean-square summing their contribution to the output.[3] Fortunately, SPICE can handle noise calculations, provided that the passive and active elements are appropriately modelled.

To develop an accurate noise model, first the existing model is modified to be essentially noiseless, then realistic noise sources are added to produce both broadband and 1/*f* noise. Calculations for the existing model revealed too much noise, due to the high resistances chosen for the gain- and the pole and zero stages, so the model was revised to generate negligible noise.

To do this required an exercise in scaling the internal impedances and currents. Instead of using 1 MΩ for the pole and zero stages, the resistance was lowered to 1 Ω. Then, to maintain unity gain, the transconductance of the voltage-controlled voltage source was increased to 1.0 mho. All sections of the model were scaled for noise except the output stage; its impedance is dictated by the device specifications. Using 1-Ω resistors, as well as a high input-stage current, leads to fictitiously large supply currents, which are furnished by supplemental fictitious supplies.

After these changes, with inherent noise in the picovolt range, noise generators are added. Figure 4 shows the generator, which comprises two diodes and two voltage sources. During a SPICE noise analysis, any semiconductor device will generate both broadband and 1/*f* noise. Diodes were chosen because they are the simplest elements to work with. By properly setting the diode model parameters pertaining to noise, any amount of broadband and 1/f noise can be modelled. The parameters are RS, the series parasitic resistance, KF, the flicker noise coefficient, and AF, the flicker noise exponent.

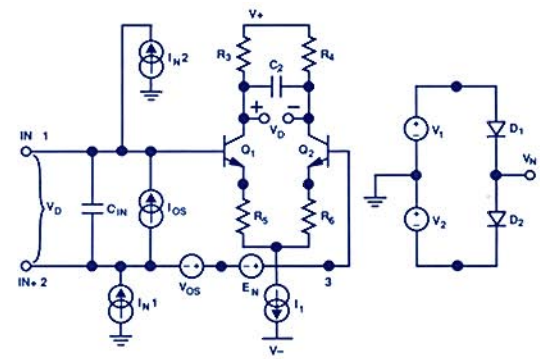


Figure 4. Noise generator and input stage.

This same topology is used for both voltage and current noise generators. A voltage-controlled voltage source introduces this noise as a voltage noise into the input stage and a voltage-controlled current source provides current noise. These sources are controlled from the junction of the two diodes—biased around ground to avoid introducing offsets into the input stage. With these simple sources the noise performance for most op amps can be modelled.

A FILTER DESIGN EXAMPLE

Filter circuits are not easy to design and analyze. Even the straightforward state-variable filter topology shown in Figure 5—which might be part of a chain of biquads making up a high-order filter—needs careful consideration. The effects of amplifier characteristics on system performance and loop stability are not easy to predict, especially as the filter's cutoff frequency and/or Q are increased. Since the circuit might have to filter random noise from an input signal, noise generated in the filter is of interest.

This example concerns a bandpass filter with a center frequency of 160 kHz, a *Q* of 1, a gain of 20 dB, and added output noise less

than 100 nV/√Hz at 160 kHz. The center frequency is set ideally by $1/(2\pi\sqrt{R_aR_bC_cC_d})$, where R_3C_1 and R_4C_2 are the frequency-determining components. Choosing the resistance values to be 10 kΩ, C_1 and C_2 are calculated to be 100 pF. The gain is set by R_2/R_1; with R_2 = 10 kΩ, R_1 becomes 1 kΩ. These values are a good starting point for the filter circuit, and by plugging in 10 kΩ for the remaining resistances, the circuit can be simulated for functionality. OP-27s are initially chosen because of their low noise performance, good (but as it turns out, not good enough) bandwidth, and unity-gain stable operation.

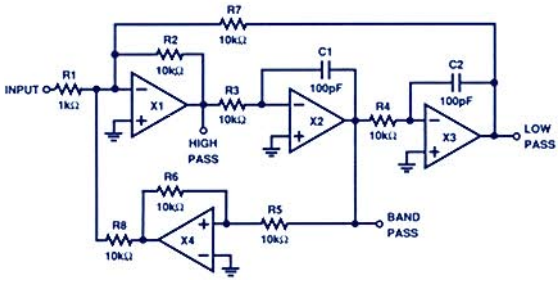


Figure 5. State-variable filter.

Figure 6 shows the resulting plot of the simulated bandpass output. Notice that the gain is slightly higher than 20 dB and the center frequency is 200 kHz, not 160 kHz; also, the high-frequency rolloff is much faster than theory predicts for a biquad. A high Q setting could account for the higher gain, but not the incorrect frequency and fast rolloff. In fact, the gain-bandwidth product (GBWP) of X1, the summing OP-27, is the limiting factor. At a gain of >20 dB, the OP-27's bandwidth is <800 kHz, which is insufficient to build a filter with an easily predictable center frequency of the desired value. However, by substituting other op amps in the ADSpice library, a suitable one with higher bandwidth is easily found. For example, the OP-61, with a 200-MHz GBWP, has ample bandwidth at an inverting gain of 10. A simulation of a circuit using this op amp gives the correct center frequency and the predictable rolloff (Figure 7).

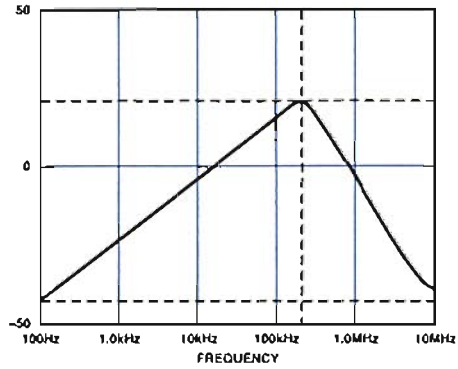


Figure 6. Bandpass output with OP-27 input amplifier.

The Q of the filter is not as simple to calculate, so why not let SPICE do the work? By adjusting the value of R5 in the simulation, we can try different values for Q. Figure 7 shows sweeps of the transfer function amplitude for five different resistance values. Checking the −3-dB bandwidth with differing values of R_5 reveals that Q = 1 when R_5 = 10 kΩ.

Note that if the design had mandated the use of a particular amplifier (for example, the OP-27), the ability to explore with SPICE would have allowed us to seek appropriate *revised* values of capacitance to set the center frequency more accurately and of R_5 to set the Q—and it would also allow the sensitivity to the amplifier's open-loop bandwidth to be checked.

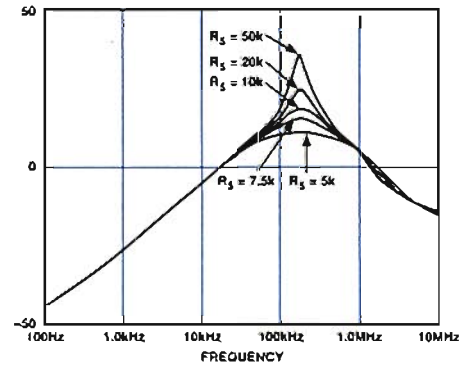


Figure 7. Adjusting the Q of the revised filter.

Once a circuit design is evaluated in SPICE, a breadboard needs to be built to verify the results. It is important to realize that SPICE cannot reveal every nuance and behavior of the circuit.

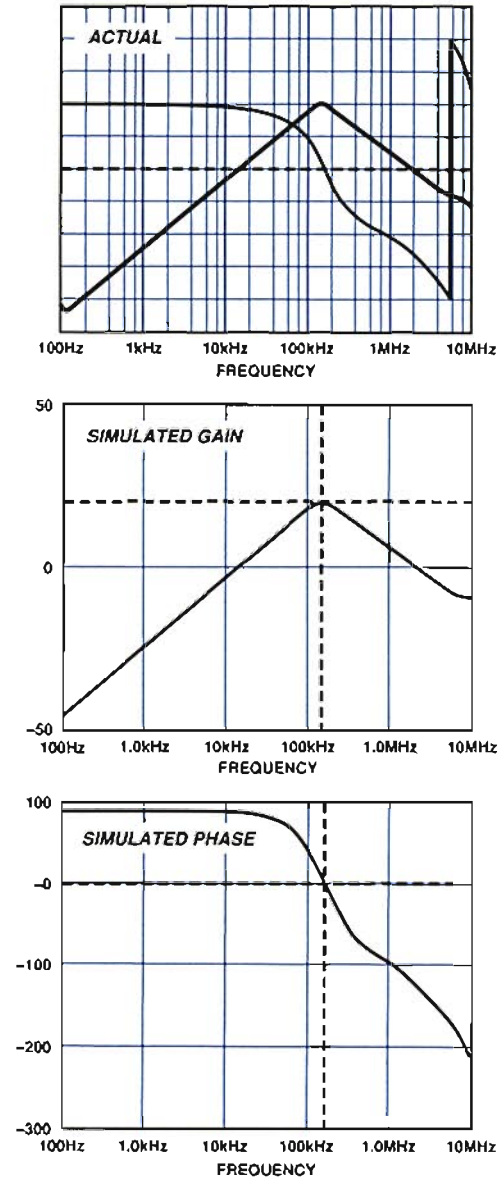


Figure 8. Gain and phase plots—actual (above) and simulated results.

Parasitic capacitances and inductances on the traces and passive components as well as limitations in the SPICE models may cause problems that will only be revealed on a breadboard. Thus, the design must be verified in the real world.

Figure 8 compares the measured gain and phase of the actual circuit with the SPICE simulation. The simulation agrees closely with the actual results: the gain is correct to within 0.1 dB and the phase within 0.1 degrees. This close agreement can be jointly attributed to both the accuracy of the ADSpice model and careful construction of the breadboard to minimize parasitics.

Another critical test is to measure the pulse response of the filter. Figure 9 shows the actual and predicted performance of the bandpass output with a 100-mV p-p square-wave input. Again, the SPICE analysis is almost identical. The height, period, and damping of the transient pulse are accurately predicted.

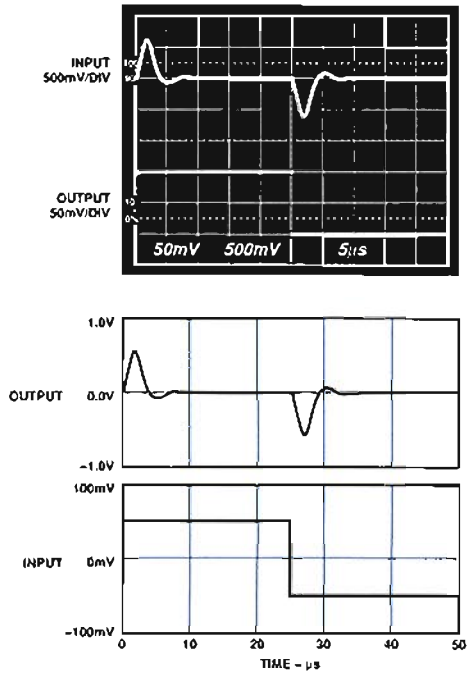


Figure 9. Transient response of bandpass output.

Finally, the noise of the circuit is analyzed. Figure 10 shows the SPICE analysis of the output noise spectral density, which peaks at 80 nV/$\sqrt{\text{Hz}}$. A spectrum analyzer measurement of the actual circuit gives results differing by only ±1 nV/$\sqrt{\text{Hz}}$. The SPICE

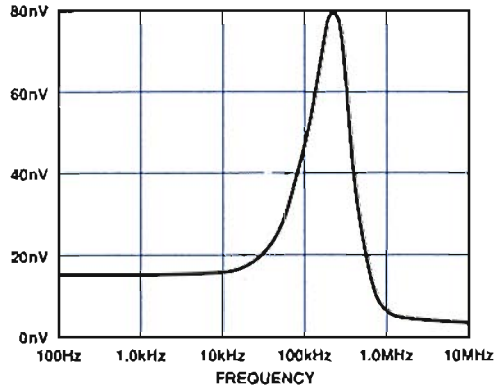


Figure 10. Noise spectral density of output, nV/$\sqrt{\text{Hz}}$.

*Simulations and graphic outputs are produced using PSpice simulation software from MicroSim Corporation, Irvine, California.

analysis can also reveal the sources of noise in the circuit; each element's noise contribution is printed in the output file—pointing the way to improving performance. For this circuit, the output file shows that R1 and amplifier X1 contribute most of the noise. To lower the noise R_1 can be reduced by a factor of 2 (along with R_2, R_7, and R_8 to maintain the ratios); this reduces the peak noise to 70 nV/$\sqrt{\text{Hz}}$, a reduction of more than 1.1 dB.

SPICE can also help to determine the total noise, and from that, the signal to noise ratio (SNR). For a given bandwidth, the total noise is determined by squaring and integrating the spot noise function with respect to frequency, then taking the square root. This is easily done using graphing software such as MicroSim* Probe, which does all the work (Figure 11). Using the equation at the bottom of the plot, the noise is integrated over a 10-MHz bandwidth, giving a total of 44.3 µV rms, from which the SNR can be calculated. Using a crest factor of 6, peak-to-peak noise is 260 µV (0.27% probability of higher peaks).

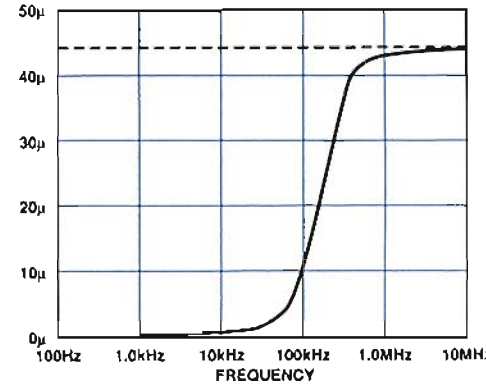


Figure 11. Total integrated noise as a function of bandwidth.

As this example shows, the ADSpice models provide engineers with a powerful tool for designing circuits with SPICE. AC and transient responses can be checked straightforwardly and quickly; and the accuracy of the model can lead to accurate simulation results. In addition, the flexibility of easily changing op amps and component values facilitates optimizing the design and can save a lot of time in the breadboard phase.

LIBRARY

Analog Devices offers a comprehensive ADSpice macromodel library in a 5 1/4" DOS-compatible diskette free of charge. Currently, a total of 176 device models are available. To request a free copy, phone your local sales office, contact the ADI literature center at 1 (800) 262-5643, or use the reply card. Circle 26

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[1] D. F. Bowers and M. Alexander, "New SPICE Compatible Op-amp Model Boosts AC Simulation Accuracy," *EDN*, Vol. 35, no. 4, pp. 143–54, February 15, 1990. Reprinted as AN-138; for a copy circle 27

[2] Boyle, Graeme R, et al, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid State Circuits*, Vol. sc-9, no. 6, December 1974.

[3] Erdi, Wong, *et al*, "AN-15 Minimization of Noise in Operational Amplifier Applications," originally in PMI *Linear and Conversion Applications Handbook, 1986*; to be included in Analog Devices' *Audio-Video Product Reference Manual*. For a copy when available, circle 28

ANALOG DEVICES NAMES NEW FELLOWS

Analog Devices has named two new Fellows during 1991, **Derek Bowers** and **Wyn Palmer**. ADI Fellows constitute the highest levels of a Parallel Ladder program, started in 1980 and developed to clarify and enhance the career opportunities for our technical contributors. The program is intended to provide the same career potential for technical contributors as for managers, in terms of compensation, recognition, and impact on the corporation. With it, we aspire to retain and motivate lifelong career technologists as a cornerstone to continued success.

Our program recognizes that technical contributors expand their influence and contributions to the company as their careers progress, and that their contributions are equivalent in scope to those of the professionals who choose management careers. The equivalent career potentials can be seen in the table.

Technical Contributor	Manager
Fellow	VP/General Manager/Director
Senior Staff Engineer	Product-Line Manager
Staff Engineer	Functional Manager
Senior Product Engineer	Engineering Supervisor

A Fellow combines enough of these roles: innovator, mentor, entrepreneur, consultant, engineering manager, organizational bridge, teacher, publisher, gatekeeper, and ambassador, to impact the corporation in an important way.

Nominations for Fellow are initiated by the technical community, spearheaded by the current Fellows. The roster of Fellows includes both design and process engineers—signifying the importance of our technologies in the progress of the company. In general, according to Chairman and CEO Ray Stata, "We are looking for innovation, for past and future contributions, and for people we can look at and say that we want our other technical people to aspire to be like them." As of today, our Fellows are:

Derek Bowers (1991)
Lew Counts (1984)
Peter R. Holloway (1985)
Jack Memishian (1980)
Michael P. Timko (1982)
Mike Tuthill (1988)
A. Paul Brokaw (1980)
Barrie Gilbert (1980)
Jody Lapham (1988)
Wyn Palmer (1991)
Robert W. K. Tsang (1988)

DEREK BOWERS

When Analog Devices acquired Precision Monolithics, Inc., in 1990, it was our extreme good fortune to be able to welcome Derek F. Bowers to our staff. A decade earlier, he had transferred to Santa Clara as a design engineer, after having joined PMI as a Field Applications Engineer in the United Kingdom in 1978. Promoted to PMI Fellow in 1986, he became a Staff Vice President (Senior Fellow) at PMI in 1987.

Derek has designed many products for PMI, including the OP-200 and OP-400 dual and quad op amps, the AMP-01 precision instrumentation amplifier, the OP-270 low-noise dual and OP-490 micropower quad op amps, and sections of the SSM-2125 Pro Logic Surround-Sound decoder chip (*Analog Dialogue* 25-1).

More are in the works. According to Ray Stata, "Among his designs are many products that have pushed the state of the art in both design and process in audio, data acquisition, op amps, references, and other areas." In addition to his design, device, and programming contributions, Derek has acted as the senior mentor for the design staff at PMI.

He has been granted many patents, with more pending. He has delivered numerous papers at conferences, published them in a variety of technical society journals, and written many articles for a the trade press. He also wrote a chapter for the book, *Analogue IC design: the current mode approach* (ed. Tomazou, Lidgey, and Haigh, published by Peter Peregrinus 1990). A Senior Member of IEEE, he serves on a Bipolar Circuits and Technology committee.

A native of the United Kingdom, Derek received a B.Sc. degree in physics and mathematics from Sheffield University and has been accepted as a Ph.D. candidate by Oxford Polytechnic.

WYN PALMER

Wyn Palmer joined Analog Devices in 1984 as a Design Engineer in the Linear Operating Group at Analog Devices Semiconductor, Wilmington, MA, and within a short time had set a blistering pace of circuit development that established Analog Devices in two new product areas: high-speed-and-accuracy complementary-bipolar (CB) op amps (*Analog Dialogue* 22-2) and analog signal processors for read-write channels of hard-disk drives (22-1).

He designed the AD847 high-speed low-power op amp—and other op amps in the AD84X CB series, the AD891 50-Mb/s rigid-disk data qualifier, and (with Fellow Lew Counts) the AD736 and AD737 new-generation rms-to-dc converter chips. He has also collaborated with other designers or managed projects for numerous other products, such as the AD790 precision comparator.

In designing these new products, he has developed new circuit architectures and cell-based designs and substantially influenced process development—especially complementary bipolar and AB-CMOS, an advanced bipolar-CMOS process. He has also influenced the development of modelling and mixed-mode simulation.

Like Derek, Wyn comes to us from the UK, where he obtained a BSEE with honors from the University of Leeds and an MSEE in Control Engineering from the University of Southampton.

Before joining Analog Devices, he was a senior principal engineer for storage systems at Digital Equipment Corp. (DEC), where he was responsible for the technical leadership of the read/write and servo developments for the SABRE project. Before that, Wyn spent two years at Data General as Manager of their Mass Storage Advanced Technology department. Earlier he was a senior hardware engineer at Burroughs and worked on a variety of scientific communication satellites at Marconi, where he served as a project leader on the UK5 scientific satellite for infrared astronomy.

Ask The Applications Engineer—10

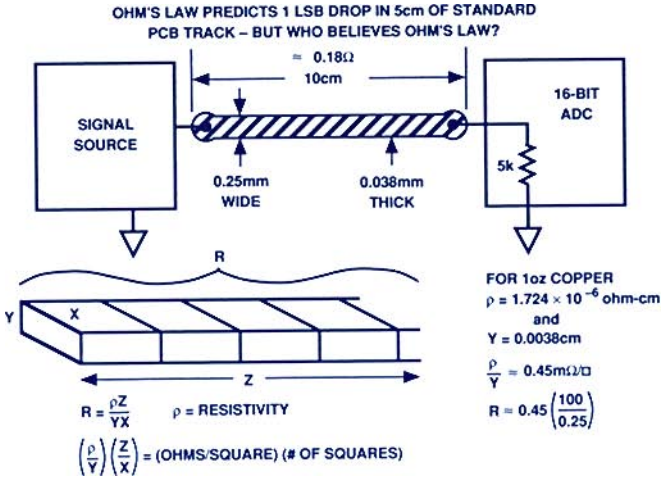
by James Bryant

Q. *In the last issue of Analog Dialogue you told us about some of the problems of a simple resistor.* [More will appear in a future issue.] *Surely there must be some component that behaves exactly as I expected it to. How about a piece of wire?*

A. Not even that. You presumably expect your piece of wire or length of PC track to act as a conductor. But room-temperature superconductors have not yet been invented, so any piece of metal will act as a low-valued resistor (with capacitance and inductance, too) and its effect on your circuit must be considered.

Q. *Surely the resistance of a short length of copper in small-signal circuits is unimportant?*

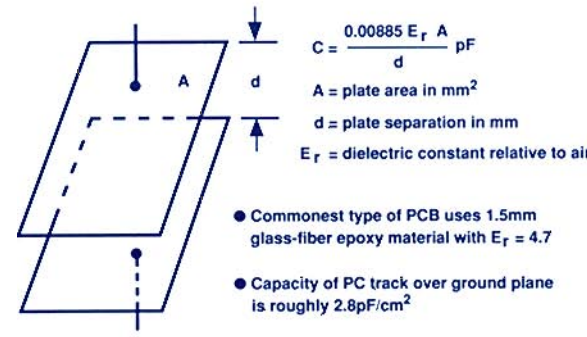
A. Consider a 16-bit a/d converter with 5-kΩ input impedance. Suppose that the signal conductor to its input consists of 10 cm of typical PC track—0.25 mm (0.010") wide and 0.038 mm (0.0015") thick. This will have a resistance of approximately 0.18 Ω at room temperature, which is slightly $<2 \times 2^{-16}$ of 5 kΩ; this introduces a gain error of 2 LSB at full scale.



One might argue that the problem would be reduced if PC tracks were made wider—and indeed, in analog circuitry it's almost always better to use wide tracks; but many layout drafters (and PC Design programs) prefer minimum-width tracks for signal conductor. In any case it's especially important to *calculate* the track resistance and its effect in every location where it might cause a problem.

Q. *Doesn't the capacitance of the extra width of track to metal on the board's underside cause a problem?*

A. Rarely. Although the capacitance of PC tracks is important (even in circuits designed for low frequencies, since LF circuits can oscillate parasitically at HF) and should always be evaluated, the extra capacitance of a wider track is unlikely to cause a problem if none existed previously. If it is a problem, small areas of ground plane can be removed to reduce ground capacitance.



Q. *Hold it! What's a ground plane?*

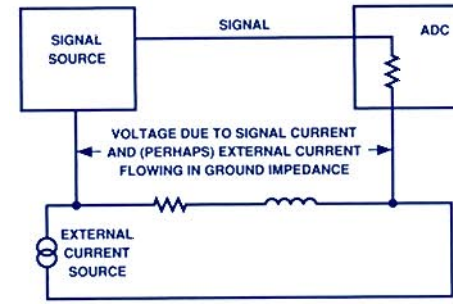
A. If one entire side of a PCB (or one entire layer, in the case of a multi-layer PCB) consists of continuous copper which is used as ground this is known as a "ground plane." It will have the least possible resistance and inductance of any ground configuration. If a system uses a ground plane, it is less likely to suffer ground noise problems.

Q. *I have heard that ground planes are hard to manufacture.*

A. Twenty years ago there was some truth in this. Today improvements in PC adhesives, solder resists and wave-soldering techniques make the manufacture of ground-plane PCB's a routine operation.

Q. *You say that a system using a ground plane is "less likely" to suffer ground noise problems. What remaining ground noise problems does it not cure?*

A. The basic circuit of a system having ground noise is shown in the diagram. Even with a ground plane the resistance and inductance will not be zero—and if the external current source is strong enough it will corrupt the precision signal.

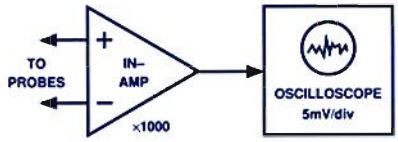


The problem is minimized by arranging the PCB so that high currents do not flow in regions where ground voltages can corrupt precision signals. Sometimes a break or slot in a ground plane can divert a large ground current from a sensitive area—but breaks in a ground plane can also reroute signals into sensitive areas, so the technique must be used with care.

Q. *How do I know what voltage drops are present in a ground plane?*

A. They should generally be measured; however, it is sometimes possible to calculate them from the resistance of the ground

plane material (standard 1 oz copper has resistance of 0.45 mΩ/square) and the length through which currents flow, but the calculation can be complicated. At DC and low frequencies (dc-50 kHz), voltage drops can be measured with an instrumentation amplifier such as the AMP-02 or the AD620.*



The amplifier is set to a gain of 1,000 and connected to an oscilloscope with a gain of 5 mV/div. The amplifier may be powered from the same supply as the circuit being tested—or from its own supply—but the grounds of the amplifier, its supply if separate, and the oscilloscope must be connected to the power ground of the circuit under test at the power supply.

The voltage between any two points on the ground plane may then be measured by applying the probes to those points. The combination of the amplifier gain and oscilloscope sensitivity give a measurement sensitivity of 5 μV/div. Amplifier noise will swell the oscilloscope trace to a band about 3 μV wide but it is still possible to make measurements with about 1-μV resolution—sufficient to identify most low-frequency ground noise problems; and identification is 80% of a cure.

Q. *Are there any cautions about performing this test?*

A. Any alternating magnetic fields which thread the probe leads will induce voltages in them. This can be tested by short-circuiting the probes together (and resistively to ground to provide a bias current path) and observing the oscilloscope trace; ac waveforms observed that result from inductive pick-up may be minimized by repositioning the leads or taking steps to eliminate the magnetic field. It is also essential to ensure that the ground of the amplifier is connected to the system ground; without this connection the amplifier, with no return path for bias current cannot work; grounding also ensures that this connection does not disturb the current distribution that is being measured.

Q. *What about measuring HF ground noise?*

A. It is hard to make a suitable instrumentation amplifier with wide bandwidth, so at HF and VHF a passive probe is more suitable. This consists of a ferrite toroid (6-8 mm OD) wound with two coils of 6-10 turns each. One coil is connected to the input of a spectrum analyzer, the other to the probes, to make a high-frequency isolating transformer.

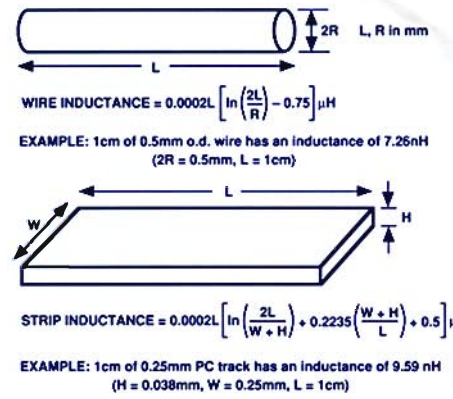
The test is similar to the LF one but the spectrum analyzer displays noise as an amplitude-frequency plot. While this differs from time-domain information, sources of noise may be easier to identify by their frequency signatures; in addition, the use of a spectrum analyzer provides at least 60 dB more sensitivity than is possible with a broadband oscilloscope.

Q. *What about the inductance of wires?*

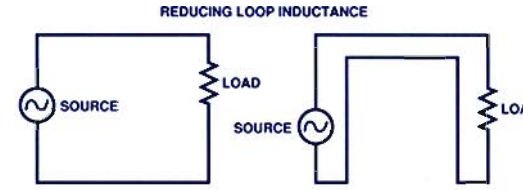
A. The inductance of wire- and PC-track leads should not be overlooked at higher frequencies. Here are some approximations for calculating the inductance of straight wires and runs.

*Use the reply card for data sheets on these amplifiers. Circle 29

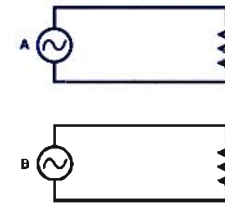
For example, 1 cm of 0.25-mm track has an inductance of 10 nH.



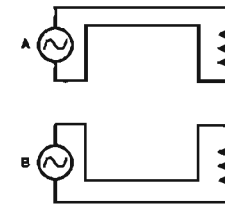
But inductive reactance is generally much less of a problem than stray flux cutting inductive loops and inducing voltages; loop area must be minimized, since voltage is proportional to it. In wired circuits this is easily done using twisted pairs.



In boards, leads and return paths should be close together; quite small changes in layout will often minimize the effect.



In this circuit, mutual inductance will couple energy from high-level source A into low-level circuit B.



Reducing area and increasing separation will minimize the effect.

Usually, all that is necessary is to minimize loop area and maximize the distance between potentially interfering loops. Occasionally magnetic shielding is required, but it is expensive and liable to mechanical damage; avoid it whenever possible.

REFERENCES

The Best of Analog Dialogue 1967-1991. Norwood MA: Analog Devices (1991), pp. 120-129, 193-195. Contains many additional references. **Circle 30**

Mixed-Signal Design Seminor Notes. Norwood MA: Analog Devices (1991). Contains additional References. See next page.

Worth Reading

BOOKS

The Best of *Analog Dialogue* 1967-1991

Reprints of items of lasting interest from 25 years of *Analog Dialogue*. Includes in chronological order application and practice articles that have been in demand—and introductions of landmark products. Paperbound 8 1/2" × 11", Table of Contents and Index: 224 pp. **Free.** Limited supply. **Circle 30**

Mixed-Signal Processing Design Seminar Notes, published by Analog Devices, Inc., 1991, 392 pp. Mixed signal processing of real-world signals and signal conditioning. *Contents:* Linear and nonlinear analog signal processing; Fundamentals of sampled-data systems; ADCs for DSP applications; DACs for DSP applications; Sigma-delta ADCs and DACs; Digital signal-processing techniques; DSP hardware; Interfacing ADCs and DACs to digital signal processors; Mixed signal processing applications; Mixed-signal circuit techniques, Index. Price $22. **Mastercard & VISA, phone (617) 461-3392, or FAX (617) 821-4273**

ADSP-21020 User's Manual A complete reference on ADI's Floating-Point DSP—for system designers and programmers. Contents: Introduction, Computation units, Program sequencing, Data address generators, Timer, Memory Interface, Instruction summary, Assembly programming tutorial, Hardware system configuration, plus appendixes on Instruction set reference, Compute operation reference, IEEE 1149.1 test access port, Data formats, Control status registers. **Free.** Limited supply. **Circle 31**

SELECTION GUIDES

DSP Product Line Cards: Two durable cards that summarize DSP Processors and Development Tools from Analog Devices: *Analog Devices' Family of DSP Processors* and *Analog Devices' DSP Development Tools*. **Free. Circle 32**

Reference Selection Guide [G1586] Tabular answers to the question "What references can I use with this converter?" **Circle 33**

SERIAL PUBLICATIONS

DSPatch—The DSP Applications Newsletter:

Number 19, Spring, 1991, 24 pp. ICASSP issue. **Circle 34**

Number 20, Summer, 1991, 20 pp. Introducing the ADSP-21020 Floating-Point Processor. Also featuring Ericsson-GE MASTR IIe base station, Nu-Metrics HI-STAR™ traffic analyzer. "How to talk analog" discusses aperture delay. And much more. **Circle 35**

Number 21 Fall, 1991, 16 pp. Featuring Saddle Point Systems Espresso Board, using ADSP-2105 for JPEG image compression. Also articles on Xing Technology's VT-Compress Software, Ixthos IXD7232 VME Board, JTAG test access port & boundary-scan testing, Numerical C and DSP/C™, and others. **Circle 36**

Analog Briefings—The Newsletter for Defense/Aerospace

Volume 7, number 2, 1991, 12 pages + 4-page insert: RADTEST℠ Data Service—first of 2 articles, plus 3-pages of insert listing products, DSP subsystems on MCM modules, Amplifiers for transducer interfacing, Class-S R/D converter, Marketing administrators, Databooks, /883 vs. SMD vs. JAN, Newly qualified products. **Circle 37**

APPLICATION NOTES

An IC amplifier user's guide to decoupling, grounding, and making things go right for a change, by Paul Brokaw (AN-202). The latest printing of this popular 8-page classic. **Circle 38**

How to reliably protect CMOS circuits against power supply overranging, by Mike Byrne. (C1499) 4 pp. Discusses power-supply overvoltaging—a common cause of electrical overstress (EOS)—and gives some simple hints on protection. **Circle 39**

RMS-to-DC converters ease measurement tasks, by Bob Clarke, Mark Fazio, and Dave Scott. (E1519) 12 pp. How rms-to-dc converters work, How to select an rms-to-dc converter, Theory and Applications of the AD736 & AD737, Applications of the AD637. **Circle 40**

Using the AD650 VFC as a frequency-to-voltage converter, by Steve Martin. (E1539) 6 pp. F/V architecture and operation, component selection, design example, tradeoff between ripple and response time. **Circle 41**

Using multiple AD1334s [4-channel 12-bit sampling ADCs] in many-channel synchronous sampling applications, by Stephan Goldstein. (E1435) 2 pp. Taking advantage of the tight group-delay specifications of the four input sample-holds in the AD1334 to expand the number of input channels. The necessary hooks already exist in the internal controller. **Circle 42**

Interfacing two 16-bit AD1856 {AD1851} audio DACs with the Philips SAA7220 digital filter, by Kevin Greene (AN-207) 4 pp. How to combine a low-distortion-and-noise 16-bit DAC with a 4× oversampling digital filter to yield a system with very low THD+N and excellent SNR. **Circle 43**

Using digitally programmable delay generators, by Allen Hill (E1518a) 6 pp. Using the AD9500 and AD9501 in programmable oscillators, pulse delays, multichannel deskewing, laser applications, and pulsewidth modulation. **Circle 44**

Considerations for selecting a DSP processor, by Bob Fine and Gerald McGuire. (E1558) 16 pp. Comparing the DSP capabilities of the ADSP-2101 and the TMS320C50, with regard to arithmetic operations, data addressing, program sequencing, and I/O handling. An example is given—a brief program for LMS adapting of FIR coefficients. **Circle 45**

REPRINTS AVAILABLE

A low-noise, low drop-out regulator for portable equipment, by James Wong, *PCIM* Magazine, May, 1990. **Circle 46**

Careful design tames high-speed op amps, by Joe Buxton, *Electronic Design*, April 11, 1991. **Circle 47**

12-bit sampling A/D [AD1674] replaces industry-standard AD574, *Electronic Products*, April, 1991. **Circle 48**

BOOKS NOTED BRIEFLY (not available from ADI)

Analog Circuit Design—Art, Science, and Personalities, edited by Jim Williams. Boston: Butterworth-Heinemann (1991). A collection of interesting articles—many describing personal experiences—by 22 contributors (ten of whom will be in some way familiar to faithful readers of these pages).

Troubleshooting Analog Circuits, by Robert A. Pease. Boston: Butterworth-Heinemann (1991). *EDN* series of articles (reviewed in *Analog Dialogue* 23-4, 1989, p. 2) expanded into book form.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS ••• New update of **ADSpice library** on diskette: 264 macromodels including first-ever multiplier model. **Circle 26** ••• 1992 update: **The Analog family of high-speed op amps Selection Guide. Circle 50**

PUBLICATIONS IN LIMITED SUPPLY (CWYLSO*) ••• "Radiation effects on advanced linear, mixed signal, and DSP products," by John Hartman, from *Thirteenth Annual Ideas in Science & Electronics Exposition and Symposium Proceedings*, IEEE (1991) ••• Richard Groshong & Stephen Ruscak, 2-part series in *Electronic Design*: "Undersampling techniques simplify digital radio" (May 23, 1991) and "Exploit digital advantages in an SSB receiver" (June 13, 1991) ••• "Optimize ADCs for enhanced signal processing" by Tom Gratzek and Frank Murden, *Microwaves & RF* (March 1991) ••• Series of application notes pertinent to nuts and bolts of hard disk drive (HDD) design: AN-225—"12-bit voltage-output DACs for single-supply 5-V and 12-V systems," AN-210—"Adding additional input channels to the AD7773/75," AN-223—"AD7575 operation with an offset ground for disk drive applications," AN-224—"Input/output level shifting with the AD7769," AN-221—"Power-down circuit cuts power to AD7769 and AD7774," AN-222—"AD7569/AD7669 operation with offset signal grounds for disk drive applications."

ERRATA AND UPDATES ••• ***Analog Dialogue*** **25-1**, page 9, paragraph above Figure 4, resistance with an aspect ratio of 4 is 2 mΩ (not 2 Ω!) ••• **AD694**: For the 0-to-20-mA range, the 4-mA on/off pin should be set at a voltage from *4 V* to Vs (was 2 V). In Figure 4 of the data sheet (using optional pass transistor), protection is required; a 50-Ω resistor in series with BOOST is suggested ••• An updated **AD7846** Specifications page is available. CWYLSO* ••• **AD9100** data sheet, several items: (1) Page 2, under Track Mode Dynamics slew rate specs are for 25°C. Over temp, they are 500 min, 700 typical. (2) Other spec changes: Pedestal sensitivity to supply, 3 mV/V (vs. 2); Bandwidth (–3-dB) 150 MHz min (vs. 160); Worst harmonic distortion (12.1 MHz, 30 MSPS, V_{OUT} = 2 Vp-p) –76 dBFS typ –70 max at T_{max}; –73 dBFS typ –68 max at T_{min}; Settling time to 1 mV 10 ns max (vs 11). (3) Page 9, "SNR vs. analog input" curve: AD9060 curve doesn't drop sharply; it passes through (40 MHz,47.5 dB), (30,49), (20,50.5), (10,53). On same page, upper right-hand chart, caption should read "Recommended R_S vs. C_{LOAD} for optimal settling times" ••• **OP-497** specs: Large-signal voltage gain for A grade, exchange specs—1200 V/mV min, 4000 typ for –55°C to +125°C, no spec for –40°C to +85°C ••• **AD736** and **AD737** data sheets, table illustrating theoretical errors in average-responding circuit for various waveforms: for undistorted triangle wave, true rms = 0.577 V, % of reading error = –3.8%; for Gaussian noise, average-responding circuit reading (AV) = 1.111 × ac average = 0.295 V, % error = –11.4%; for rectangular pulse train, (AV) = 0.278 V and 0.011 V, % error = –44% and –89% at crest factors of 2 and 10 [note that highest CF specified for the devices is 5] ••• Revised **ADSP-2105** data sheet is available (C1463a). **Circle 51** ••• **AD9006/16** data sheet, **AD9006** pin designations: Pin 42 should be labeled NC ••• **AD2S81A/82A** data sheet, Fig. 10, and 2S80, **AD2S80A** data sheets, Figure 8, show an erroneous connection: REF LOW should be connected to pin 5, not pin 6, for best results ••• **AD9712/AD9713** d/a converters: Potpourri in Analog Dialogue 25-1 discussed a PSRR-reduction circuit; if you plan to use it, please reverse connections to the AD589 reference ••• **AD9005A** has replaced the **AD9005**; the AD9005A data sheet is available (C1511). **Circle 52** ••• Model **AD1154** data sheet revision: Droop rate specs for AD1154AW/BW are changed to 0.2/0.1 µV/µs typical @ 25°C, 0.7/0.35 µV/µs max @ 25°C, and 5/2.5 µV/µs typical at +85°C ••• **AD28msp02** Linear Codec is available in a 28-pin SOIC package; the pinout is shown on a data-sheet addendum. CWYLSO* ••• **AD7237/AD7247** is available in a 24-pin SOIC package. For an updated data sheet including this package (C1324a), **Circle 53** ••• **1990/91 Linear Products Databook**: Figure R-16 on page 20-32 should have a "B" dimension of 0.150/0.157 ••• The **AD1864** is now available in a 28-pin PLCC package; a new data sheet is available (C1405b). **Circle 54.**

PRODUCT NOTES (CWYLSO* for details) ••• **CEG** is one of many systems that give pretty pictures on a PC—but *only CEG* gives smooth lines and text under existing VGA. The new version of Bitstream FaceLift for Windows will produce sharp, clean antialiased fonts when Analog Devices CEG DACs are used ••• A **CEG demo disk** is available for VGA cards with 66-MHz CEG chips ••• **ADV476** RAM-DAC is now available in an 80-MHz version for 72-Hz VGA refresh rate in 1024×768 mode (Vesa standard) ••• **AD664A and B** are now available in 44-pin J-Leaded Chip Carrier (JLCC) and 28-pin plastic DIP packages ••• **ADSP-2101** full-featured **Emulator** (ADDS-2101-ICE) now operates at 16.67 MHz, allowing test and debug of ADSP-2101-66 processors at full speed ••• **AD694** is now available in SOIC ••• The **AD586MN** +5-V high-accuracy reference is now available...2 mV initial error, 2 ppm/°C (0 to +70°C); also the AD586LR: 2.5 mV & 5 ppm/°C ••• **Release 3.1 Development software** now supports **ADSP-2100A, -2101, -2105, -2111, and ADSP-21msp50** processors and is currently available for IBM-PC (DOS), Sun, and VAX ••• Look into ADI's **custom hybrid/multi-chip-module** technology for high functionality in a small footprint ••• **RMS-to-dc converters: AD536A** is available in cerdip; **AD637** in SOIC ••• **Instrumentation amplifier: AD524** is now available in SOIC ••• The **AD9005** ADC, now with a thin metal plate along its bottom, has 0.210" (min) pins ••• The AD9901 phase discriminator is suitable principally for PLLs with limited tuning ranges, since it can lock on odd harmonics of its reference frequency ••• **AD9058** dual-8-bit 50-MSPS ADC's price has been reduced.

WORKSHOPS AND SHOWS ••• **DSP workshops in 1992** will be held: in **Norwood MA** March 11-13 and June 10-12; in **Campbell CA** January 28-30; and in **Antwerp, Belgium** February 19-21. CWYLSO* ••• Visit us at these shows: **IEEE ICASSP '92** in San Francisco CA, March 23-26; **Comdex Spring '92** in Chicago IL, April 6-9; and **AES (Europe) in Vienna, Austria**, March 24-27.

MILITARY ROLL CALL (CWYLSO* for details) ••• Ask about advanced linear and mixed-signal products available to **Class S** ••• New /883B versions are available in these product families: **AD766** 16-bit DSP DACPORT™; **AD745** (high speed) and **AD743** lowest-noise op amps; **AD734** 10-MHz analog multiplier; **AD678** 200-ksps fast 12-bit sampling ADC; **AD704** low-offset-and-bias-current op amp, a direct upgrade for LT1014MH/883B; **AD9500 and AD9501** programmable digital delay generators; **AD664** quad 12-bit DAC; **AD9048** 8-bit, 35 MSPS ADC ••• **AD674B and AD774B** 12-bit ADCs ••• The **AD640** 120-MHz, 45-dB log amp is now available in chip form in T grade (MIL-temp operation). DIP and LCC versions are available to DESC drawing 5962-90955 ••• Radiation test results, periodically updated, are available in ADI's **RADTEST**^{SM} **data service.**

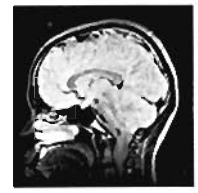
PATENTS RECEIVED ••• **5,008,671** to Michael G. Tuthill for High-speed digital-to-analog converter with BiMos cell structure ••• **5,010,297** to Douglas W. Babcock for Automatic test equipment with active load having high-speed Inhibit-mode switching ••• **5,010,337** to Shinichi Hisano, Apparaian Ganesan, and Thomas S. Guy for High-resolution d/a converter operable with single supply voltage ••• **5,021,120** to Roy V. Buck and Darrell P. Adams for Process for etching patterned substrates ••• **5,026,667** to Carl M. Roberts, Jr., for Producing integrated circuit chips with reduced stress effects ••• **5,027,085** to Lawrence M. DeVito for Phase detector for phase-locked-loop clock recovery system ••• **5,030,849** to A. Paul Brokaw for Monolithic ratiometric temperature measurement circuit ••• **5,036,298** to John F. Bulzachelli for Clock recovery circuit without jitter peaking ••• **5,036,322** to Jeffrey Barrow, William J. Pratt, and Henry T. Tsuei for Digital-to-analog converters with improved linearity ••• **5,039,945** to Spencer L. Webb for Single winding magnetometer with automatic distortion compensation ••• **5,041,795** to Derek F. Bowers for Three-terminal operational amplifier and applications thereof ••• **5,043,657** to Bruce E. Amazeen and Mark M. Martin for Marking techniques for identifying integrated circuit parts at the time of testing ••• **5,043,675** to Barrie Gilbert for Difference amplifier employing input attenuator network and powered by a single polarity power supply ••• **5,043,732** to David H. Robertson, Peter Real, and Christopher W. Mangelsdorf for Analog-to-digital converter employing a pipeline multi-stage architecture ••• **5,053,653** to Derek F. Bowers and Douglas Smith for JFET analog switch with gate current control ••• **5,055,723** by Derek F. Bowers And Douglas Smith for JFET analog switch with gate current control ••• **5,065,214** to Jerome F. Lapham and Brad W. Scharf for Integrated circuit with complementary junction-isolated bipolar transistors.

*CWYLSO: Check with your local Analog Devices sales office.

IN THE LAST ISSUE

Volume 25, Number 1, 1991, 28 Pages

Here are just a few places where you'll find components from Analog Devices.



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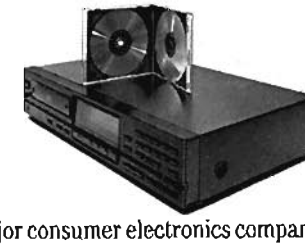

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